IEEE ICCD 2005
CALL FOR PAPERS

October 2 — 5, 2005
Doubletree Hotel, San Jose CA.

Sponsored by the IEEE Computer Society and IEEE Circuits and Systems Society, in cooperation with the IEEE Electron Devices Society

IEEE International Conference on Computer Design

IMPORTANT DATES
Submission deadline : May 6th
Notification deadline : June 24th
Final manuscript : July 22nd

http://www.iccd-conference.org

The International Conference on Computer Design encompasses a wide range of topics in the research, design, and implementation of computer systems and their components. ICCD's multi-disciplinary emphasis provides an ideal environment for developers and researchers to discuss practical and theoretical work covering system and computer architecture, verification and test, design and technology, and tools and methodologies.

The theme for the 2005 ICCD conference is:

Toward the 10 Billion Transistor Chip - Technologies and Applications for Extremely Large Integrated Systems.

Submitted papers consistent with this theme are encouraged. Authors are invited to submit technical papers in accordance to the author's instructions describing original work in one of the following areas:

Computer Systems Design and Applications
Advanced computer architecture for general and application-specific enhancement; Modeling and performance analysis; Support for operating systems and languages; Memory hierarchy; System design methods for uni- and parallel-processors.

Processor Architecture
Microarchitecture design techniques: instruction-level parallelism, pipelining, caching, branch prediction, multithreading, computer arithmetic; Techniques for low-power; secure, and reliable processor designs; Embedded, network, system-on-chip, and application-specific processor design; real-life design challenges: case studies, tradeoffs and post-mortems.

Logic and Circuit Design
Circuits and design techniques for digital, memory, and mixed-signal systems; Circuits and design techniques for high performance and low power; Circuits and design techniques for robustness under process variability and radiation; Design techniques for emerging process technologies; Asynchronous circuits; Signal processing and arithmetic circuits.

Tools and Methodology
High-level, logic and physical synthesis. Physical planning, design and early estimation for large circuits. Automatic analysis and optimization of timing, power and noise. Tools for multiple-clock domains, asynchronous and mixed-timing methodologies. CAD support for FPGAs, ASSPs, structured ASICs, platform-based design and networks-on-chip. Hardware description languages. Tools, methodologies and design strategies for emerging technologies (MEMs, spintronics, nano, quantum).

Verification and Test
Simulation based and formal techniques for functional design verification; Equivalency checking, property checking, theorem proving; High-level design validation; Design error debug and diagnosis; Hardware/Software validation; Fault modeling; Fault simulation and ATPG; DFT and BIST; SoC testing.

Papers describing novel methods and concepts or innovative features of new products, and focusing on the overall integration of these areas into the computer design process are of particular interest to ICCD. Papers may be accepted as either regular papers or as short papers. All papers will be presented during parallel technical sessions, and will be included in a published proceedings. At least one author of the paper must register for and attend the conference.

Proposals for embedded tutorials and panel discussions are also solicited, and should be sent to:

Pranav Ashar, ashar@realintent.com

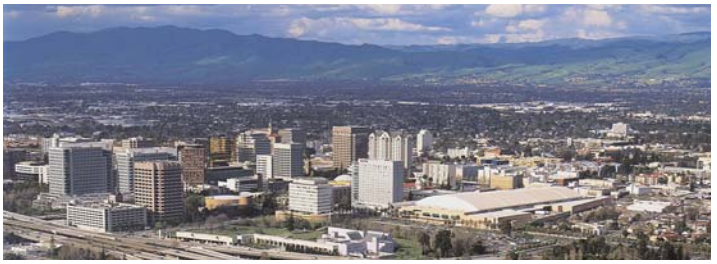
Instructions to Authors
The submitted manuscript should closely reflect the final paper as it will appear in the Proceedings, which will be a maximum of eight pages in IEEE double column format. (Papers greater than six pages will incur an extra page charge.) The international review committee will give preference to papers that (excluding references, figures, and tables) do not exceed 3000 words to clearly present the work, methods, results, originality, significance, superiority, and applications of the techniques discussed.

Electronic Submission
Authors should plan on formatting their papers in Postscript format. Details on the electronic submission are available at :

http://www.iccd-conference.org.

Questions about the submission procedure may be sent to:

Pranav Ashar, ashar@realintent.com



ICCD 2005 ORGANIZING COMMITTEE

General Chair
Ed Grochowski, Intel Corporation

Technical Program Chair
Pranav Ashar, Real Intent Corporation

Vice Program Chair
Dirk Timmermann, University of Rostock, Germany

Publicity Chair
Kee Sup Kim, Intel Corporation

Publication Chair
Peter-Michael Seidel, Southern Methodist University

Finance and Special Sessions Chair
Kevin Rudd, Intel Corporation

Computer Systems Design and Applications Track
Srinidhi Varadarajan, Virginia Tech
Godmar Back, Virginia Tech

Processor Architecture Track
David Brooks, Harvard University
Michael Gschwind, IBM Research

Logic and Circuit Design Track
Michael Orshansky, University of Texas at Austin
Vivek De, Intel Corporation

Tools and Methodology Track
Steven Nowick, Columbia University
Igor Markov, University of Michigan

Verification and Test Track
Alan Hu, University of British Columbia
Alex Orailoglu, UC San Diego