ADVANCE PROGRAM

Monday, October 8			
8:00-8:30	Registration		
8:30-9:00	Welcome Remarks		
9:00-10:00	Keynote Talk: Paul Dent		
10:00-10:30	Break		
10:30-12:00	Session 1.1 -- Signal Processing Circuits (90 min) • Twiddle Factor Transformation for Pipelined FFT Processing (In-Cheol Park, WonHee Son and Ji-Hoon Kim) • Contention-Free Switch-Based Implementation of 1024-point Radix-2 Fourier Transform Engine (Hani Saleh, Bassam Mohd, Adnan Aziz and Earl Swartzlander) • A speed-area optimized architecture for Full Search Block Matching with applications in high-definition TVs (HDTV) (Santosh Ghosh and Avishek Saha)	Session 1.2 -- Advances in Verification (90 min) • Bounded Model Checking of Embedded Software in Wireless Cognitive Radio Systems (Nannan He and Michael Hsiao) • Application of Symbolic Computer Algebra to Arithmetic Circuit Verification (Yuki Watanabe, Naofumi Homma, Takafumi Aoki and Tatsuo Higuchi) • Continual Hashing for Efficient Fine-grain State Inconsistency Detection (Jae W. Lee, Myron King, and Krste Asanovic) (Short Paper) • Automatic SystemC TLM Generation for Custom Communication Platforms (Lochi Yu and Samar Abdi) (Short Paper)	Session 1.3 -- Novel Memory and Communication Subsystems (90min) • Improving Cache Efficiency via Resizing + Remapping (Subramanian Ramaswamy and Sudhakar Yalamanchili) • Exploring DRAM Cache Architectures for CMP Server Platforms (Li Zhao, Ravi Iyer, Ramesh Illikkal and Don Newell) • A 4.6Tbits/s 3.6GHz Single-Cycle NoC Router with a Novel Switch Allocator in 65nm CMOS (Amit Kumar, Partha Kundu, Arvind Singh, Li-Shiuan Peh and Niraj Jha)
12:00-1:30	Lunch		
1:30-3:30	Session 2.1 -- Variation Aware Design Methodologies (120 min) • Analytical Thermal Placement for VLSI Lifetime Improvement and Minimum Performance Variation (Andrew Kahng, Sung-Mo Kang, Wei Li and Bao Liu) • Voltage Drop Reduction For On-chip Power Delivery Considering Leakage Current Variations (Jeffrey Fan, Ning Mi and Sheldon Tan) • On Modeling Impact of Sub-Wavelength Lithography on Transistors (Aswin Sreedhar and Sandip Kundu) • Why We Need Statistical Static Timing Analysis (Cristiano Forzan and Davide Pandini) (Short Paper) • Statistical Timing Analysis using Kernel Smoothing (Jennifer Wong, Azahdeh Davoodi, Vishal Khandelwal, Ankur Srivastava and Miodrag Potkonjak) (Short Paper)	Session 2.2 -- Tutorial: Software-Defined Radio (SDR) Technology Mark Cummings and Todor Cooklev	

3:30-4:00	Break		
4:00-5:30	Session 3.1 -- Microarchitecture, Multiprocessors and Systems-on-chip (90 min) • A Position-Insensitive Finished Store Buffer (Erika Gunadi and Mikko Lipasti) • A Low Overhead Hardware Technique for Software Integrity and Confidentiality (Austin Rogers, Milena Milenkovic and Aleksandar Milenkovic) • Cluster-Level Simultaneous Multithreading for VLIW Processors (Manoj Gupta, Josep Llosa and Fermín Sánchez) (Short Paper) • Evaluating Voltage Islands in CMPs under Process Variations (Abhishek Das, Serkan Ozdemir, Gokhan Memik and Alok Choudhary) (Short Paper)	Session 3.2 -- FPGA Architecture and Design (90 min) • Non-arithmetic Carry Chains for Reconfigurable Fabrics (Michael Frederick and Arun Somani) • FPGA Global Routing Architecture Optimization Using a Multicommodity Flow Approach (Yuanfang Hu, Yi Zhu and Chung-Kuan Cheng) • FPGA Routing Architecture Analysis Under Variations (Suresh Srinivasan, Prasanth Mangalagiri, Yuan Xie and Vijaykrishnan Narayanan) (Short Paper) • Energy-Aware Co-processor Selection for Embedded Processors on FPGAs (AmirHossein Gholamipour, Elaheh Bozorgzadeh and Sudarshan Banerjee) (Short Paper)	Session 3.3 -- Application-Optimized Architectures (90 min) • Benchmarks and Performance Analysis for Decimal Floating-Point Applications (Liang-Kai Wang, Charles Tsen, Divya Jhalani and Michael Schulte) • Multi-Core Data Streaming Architecture for Ray Tracing (Yoshiyuki Kaeriyama, Daichi Zaitsu, Kenichi Suzuki, Hiroaki Kobayashi and Nobuyuki Ohba) • Hardware Libraries: An Architecture for Economic Acceleration in Soft Multi-Core Environments (David Meisner and Sherief Reda) (Short Paper) • Compiler-assisted Architectural Support for Program Code Integrity Monitoring in Application-specific Instruction Set Processors (Hai Lin, Xuan Guan, Yunsi Fei and Zhijie Jerry Shi) (Short Paper)
5:30-6:00			
6:00-9:00	Banquet Keynote Talk: Yale Patt		

Tuesday, October 9			
8:30-9:00	Registration		
9:00-10:00	Keynote Talk: Tom Lee		
10:00-10:30	Break		
10:30-12:00	Session 4.1 -- Special Session: Three-Dimensional Integrated Circuits • Implementing a 2-Gbs 1024-bit ½-rate Low-Density Parity-Check Code Decoder in Three-Dimensional Integrated Circuits (Lili Zhou, Cherry Wakayama, Robin Panda, Nuttorn Jangkrajarng, Bo Hu, and C.-J. Richard Shi) • Amdahl's Figure of Merit, SiGe HBT BiCMOS, and 3D Chip Stacking (Phil Jacobs, Aamir Zia, Okan Erdogan, Paul Belemjian, Peng Jin, Jin Woo Kim, Mike Chu, Russ Kraft, and John F. McDonald) • Scan Chain Design for Three-dimensional Integrated Circuits (3D ICs) (Xiaoxia Wu, Paul Falkenstern, and Yuan Xie)	Session 4.2 -- Invited Session: Industry Challenges in Wireless Communication • Challenges and Prospects of SDR for Mobile Phones (Ulrich Ramacher, Infineon) • The Challenge in Testing MIMO in a Wi-Fi or WiMAX (Karsten Vandrup, LitePoint Corp.)	
12:00-1:30	Lunch		
1:30-3:30	Session 5.1 -- Cache memory architecture (I) (120 min) • Exploring the Interplay of Yield, Area, and Performance in Processor Caches (Hyunjin Lee, Sangyeun Cho and Bruce Childers) • Improving the Reliability of On-chip L2 Cache Using Redundancy (Koustav Bhattacharya, Soontae Kim and Nagarajan Ranganathan) • Reducing Leakage Power in L2 Caches (Houman Homayoun and Alex Veidenbaum) (Short Paper) • Two-level Data Prefetching (Fei Gao, Hanyu Cui and Suleyman Sair) • Cache Replacement Based on Reuse-Distance Prediction (Georgios Keramidas, Pavlos Petoumenos and Stefanos Kaxiras) (Short Paper)	Session 5.2 -- Novel Techniques in Physical Design (120 min) • Constraint Satisfaction in Incremental Placement with Application to Performance Optimization under Power Constraints (Huan Ren and Shantanu Dutt) • Fine Grain 3D Integration for Microarchitecture Design Through Cube Packing Exploration (Yongxiang Liu, Yuchun Ma, Eren Kursun, Glenn Reinman and Jason Cong) • Whitespace Redistribution For Thermal Via Insertion In 3D Stacked ICs (Eric Wong and Sung Kyu Lim) • Placement and Routing of RF Embedded Passive Designs In LCP Substrate (Mohit Pathak and Sung Kyu Lim)	Session 5.3 -- Arithmetic Circuits (120 min) • A Radix--10 SRT Divider Based on Alternative BCD Codings (Alvaro Vazquez, Elisardo Antelo and Paolo Montuschi) • Hardware Design of a Binary Integer Decimal-based Floating-point Adder (Charles Tsen, Sonia Gonzalez-Navarro and Michael Schulte) (Short Paper) • A Parallel IEEE P754 Decimal Floating-Point Multiplier (Brian Hickman, Andrew Krioukov, Mark Erle and Michael Schulte) (Short Paper) • Floating-Point Division Algorithms for an x86 Microprocessor with a Rectangular Multiplier (Michael Schulte, Dimitri Tan and Carl Lemonds) • Optimized Design of a Double-Precision Floating-Point Multiply-Add-Fused Unit for Data Dependence (Gongqiong Li and Zhaolin Li)
3:30-4:00	Break		
4:00-5:45	Session 6.1 -- Reliability and fault tolerance (105 min) • Low-Cost Run-time Diagnosis of Hard Delay Faults in the Functional Units of a Microprocessor (Sule Ozev, Daniel J. Sorin and Mahmut Yilmaz) • Improving the Reliability of On-Chip Caches Under Process Variations (Wei Wu, Jun Yang, Sheldon Tan and Shih-Lien Lu) • Prioritizing Verification via Value-based Correctness Criticality (Joonhyuk Yoo and Manoj Franklin) • Memory Based Computation Using Embedded Cache for Processor Yield and Reliability Improvement (Somnath Paul and Swarup Bhunia) (Short Paper)	Session 6.2 -- Novel Test Techniques (105 min) • Accurate Modeling and Fault Simulation of Byzantine Resistive Bridges (Hugo Cheung and Sandeep Gupta) • Negative-Skewed Shadow Registers for At-Speed Delay Variation Characterization (John Lach and Jie Li) • An Efficient Routing Method for Pseudo-Exhaustive Built-in Self-Testing of High-Speed Interconnects (Jianxun Liu and Wen-Ben Jone) (Short Paper) • Detecting Errors in a Polynomial Basis Multiplier Using Multiple Parity Bits for Both Inputs (Siavash Bayat-Sarmadi and M. Anwar Hasan) (Short Paper) • Modeling Soft Error Effects Considering Process	Session 6.3 --Low Power Design (105 min) • An Automated Runtime Power-Gating Scheme (Mototsugu Hamada, Takeshi Kitahara, Naoyuki Kawabe, Hironori Sato, Tsuyoshi Nishikawa, Takayoshi Shimazawa, Takahiro Yamashita, Hiroyuki Hara, Yukihito Oowaki and Toshiyuki Furusawa) • A Power Gating Scheme for Ground Bounce Reduction during Mode Transition (Ku He, Rong Luo and Yu Wang) • Dynamically Compressible Context Architecture for Low Power Coarse-Grained Reconfigurable Array

		Variations (Chong Zhao and Sujit Dey) (Short Paper)	(Yoonjin Kim and Rabi N. Mahapatra) • Post-Layout Comparison of High Performance 64b Static Adders in Energy-Delay Space (Sheng Sun and Carl Sechen) (Short Paper)
6:15-10	Off-site Trip		

Wednesday, October 10			
8:00-8:30	Registration		
8:30-10:00	Session 7.1 -- Power and thermal considerations in processor design (90 min) • CAP: Criticality Analysis for Power-Efficient Speculative Multithreading (James Tuck, Wei Liu and Josep Torrellas) • Power-Aware Mapping for Reconfigurable NoC Architectures (Mehdi Modarresi and Hamid Sarbazi-Azad) • LEMap: Controlling Leakage in Large Chip-multiprocessor Caches via Profile-guided Virtual Address Translation (Jugash Chandarlapati and Mainak Chaudhuri) (Short Paper) • Power efficient register file update approach for embedded processors (Raid Ayoub and Alex Orailoglu) (Short Paper)	Session 7.2 -- Circuit Design and Simulation (90 min) • A Technique for Selecting CMOS Transistor Orders (Ting-Wei Chiang, Wei-Yu Chen and C Y Roger Chen) • An Algorithm to Simplify Multi-Clock Edge Timing Constraints (Veerapaneni Nagbhushan and Roger Chen) • An Efficient Gate Delay Model for VLSI Design (Ting-Wei Chiang, Wei-Yu Chen and C Y Roger Chen) (Short Paper) • Fast Power Network Analysis with Multiple Clock Domains (Wanping Zhang, Ling Zhang, Rui Shi, He Peng, Zhi Zhu, Lew Chua-Eoan, Rajeev Murgai, Toshiyuki Shibuya, Noriyuki Ito and Chung-Kuan Cheng) (Short Paper)	Session 7.3 -- Simulation and Scheduling (90 min) • Statistical Simulation of Chip Multiprocessors Running Multi-Program Workloads (Davy Genbrugge and Lieven Eeckhout) • Combining Cluster Sampling with Single Pass Methods for Efficient Sampling Regimen Design (Paul Bryan and Thomas Conte) • A Novel O(1) Parallel Deadlock Detection Algorithm and Architecture for Multi-unit Resource Systems (Xiang Xiao and Jaehwan John Lee)
10:00-10:30	Break		
10:30-12:00	Session 8.1 -- Cache memory architecture (II) (90 min) • Limits on Voltage Scaling for Low Power, High Speed Caches (Mohammad Makhzan, Amin Khajeh, Ahmad Eltawil and Fadi Kurdahi) • VOSCH: Voltage Scaled Cache Hierarchies (Yiran Chen, Chengkok Koh, Hai Li and Weng-Fai Wong) • Exploiting eDRAM bandwidth with data prefetching: simulation and measurements (Valentina Salapura, Jose R Brunheroto, Fernando Redigolo and Alan Gara)	Session 8.2 -- RF and Analog Test (90 min) • Digital Calibration of RF Transceivers for I-Q Imbalances and Nonlinearity (Erkan Acar and Sule Ozev) • Fault-Based Alternate Test of RF Components (Selim Sermet Akbay and Abhijit Chatterjee) • Circuit-level Mismatch Modelling and Yield Optimization for CMOS Analog Circuits (Mingjing Chen and Alex Orailoglu)	Session 8.3 -- Synchronization and Interconnect (90 min) • A Study on Self-Timed Asynchronous Subthreshold Logic (Niklas Lotze, Maurits Ortmanns and Yiannos Manoli) • SCAFFI: An intrachip FPGA asynchronous interface based on hard macros (Julian Pontes, Rafael Soares, Ewerson Carvalho, Fernando Moraes and Ney Calazans) • Passive Compensation For High Performance InterChip Communication (Chunchen Liu, HaiKun Zhu and CK Cheng) (Short Paper) • Transparent Mode Flip-Flops for Collapsible Pipelines (Eric Hill and Mikko Lipasti) (Short Paper)
12:00-1:00	Lunch		
1:00-2:30	Session 9.1 -- Design Techniques for Emerging Technologies (75 min) • CMOS Logic Design with Independent-gate FinFETs (Anish Muttreja, Niket Agarwal and Niraj Jha) • Distributed Voting for Fault-Tolerant Nanoscale Systems (Ali Namazi and Mehrdad Nourani) (Short Paper) • Hybrid Resistor/FET-Logic Demultiplexer Architecture Design for Hybrid CMOS/Nanodevice Circuits (Shu Li and Tong Zhang) (Short Paper) • VIZOR: Virtually Zero Margin Adaptive RF for Ultra Low Power Wireless Communication (Rajarajan Senguttuvan, Shreyas Sen and Abhijit Chatterjee) (Short Paper)	Session 9.2 -- System Level and Architectural Synthesis (90 min) • Register Binding Guided By The Size Of Variables (Noureddine Chabini and Wayne Wolf) • Power Variations of Multi-Port Routers in an Application-Specific NoC Design : A Case Study (Balasubramanian Sethuraman and Ranga Vemuri) • System Level Power Estimation Methodology with H.264 Decoder Prediction IP Case Study (Young-Hwan Park, Sudeep Pasricha, Fadi J. Kurdahi and Nikil Dutt) (Short Paper) • A Novel Profile-Driven Technique for Simultaneous Power and Code-size Optimization in Microcoded IPs (Bita Gorjiara and Daniel Gajski) (Short Paper)	Session 9.3 -- Process-aware Design: Power, Thermal and Reliability (75 min) • Power Reduction of Chip Multi-Processors using Shared Resource Control Cooperating with DVFS (Ryo Watanabe, Masaaki Kondo, Hiroshi Nakamura and Takashi Nanya) • Effective Dynamic Thermal Management for MPEG-4 Decoding (Inchoon Yeo, Heung Ki Lee, Ki Hwan Yum and Eun Jung Kim) (Short Paper) • Priority-Monotonic Energy Management for Real-Time Systems with Reliability Requirements (Dakai Zhu, Xuan Qi and Hakan Aydin) (Short Paper) • Maximizing the Throughput-Area Efficiency of Fully-Parallel Low-Density Parity-Check Decoding with C-Slow Retiming and Asynchronous Deep Pipelining (Ming Su, Lili Zhou and C.J. Shi) (Short Paper)