



ICCD 2007

OCTOBER 7 — 10 2007, Resort at Squaw Creek, Lake Tahoe, California
XXV IEEE INTERNATIONAL CONFERENCE ON COMPUTER DESIGN

Sponsored by
IEEE Computer Society, IEEE Circuits and Systems Society, and IEEE Electron Devices Society

CALL FOR PAPERS **IMPORTANT DATES:** Submission Deadline: May 21, 2007, 11.59 p.m. (HST/GMT 10h)
■ Notification: July 13, 2007 ■ Camera-Ready: August 10, 2007

<http://www.iccd-conference.org>

The International Conference on Computer Design encompasses a wide range of topics in the research, design, and implementation of computer systems and their components. ICCD's multi-disciplinary emphasis provides an ideal environment for developers and researchers to discuss practical and theoretical work covering system and computer architecture, verification and test, design and technology, and tools and methodologies.

The theme for the 2007 ICCD conference is:

— Mobile and Wireless Computing Systems —

Submitted papers consistent with this theme are encouraged. Authors are invited to submit technical papers in accordance to the author's instructions describing original work in one of the following areas:

Computer Systems: Methods, Implementations, and Applications

Advanced computer architecture for general and application-specific enhancement; System design methods for uni- and parallel processors; Design methods for homogeneous and heterogeneous multi-core processor systems and system-on-chip designs; IP and platform-based designs; HW/SW-Codesign; Modeling and performance analysis; Support for security, languages and operating systems; Smart Cards; Real-time Systems; Application-specific and embedded software optimization; Optimizing and parallelizing compiler support for multithreaded and multi-core designs; Memory system and Network system optimization.

Processor Architecture

Microarchitecture design techniques for uni- and multi-core processors: instruction-level parallelism, pipelining, caching, branch prediction, multithreading, computer arithmetic; Techniques for low-power; secure, and reliable processor designs; Embedded, network, graphic, system-on-chip, application-specific and digital signal processor design; real-life design challenges: case studies, tradeoffs and post-mortems.

Logic and Circuit Design

Circuits and design techniques for digital, memory, analog and mixed-signal systems; Circuits and design techniques for high performance and low power; Circuits and design techniques for robustness under process variability and radiation; Design techniques for emerging process technologies (MEMs, spintronics, nano, quantum); Asynchronous circuits; Signal processing and arithmetic circuits, and circuits for graphic processor design.

Electronic Design Automation

High-level, logic and physical synthesis. Physical planning, design and early estimation for large circuits; Automatic analysis and optimization of timing, power and noise; Tools for multiple-clock domains, asynchronous and mixed timing methodologies; CAD support for FPGAs, ASSPs, structured ASICs, platform-based design and networks-on-chip; DfM and OPC methodologies; Tools, methodologies and design strategies for emerging technologies (MEMs, spintronics, nano, quantum).

Verification and Test

Functional, transaction-level, RTL, and gate-level modeling and verification of hardware designs; Simulation-based and formal techniques for functional design verification; Dynamic simulation, equivalence checking, formal verification, model and property checking, and theorem proving; high-level design validation; hardware emulation, modeling languages, assertion-based verification, coverage-analysis, constrained-random test generation; design error debug and diagnosis; Hardware/Software validation; Fault modeling; Fault simulation and ATPG; Fault tolerance; DFT and BIST; SoC verification.

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