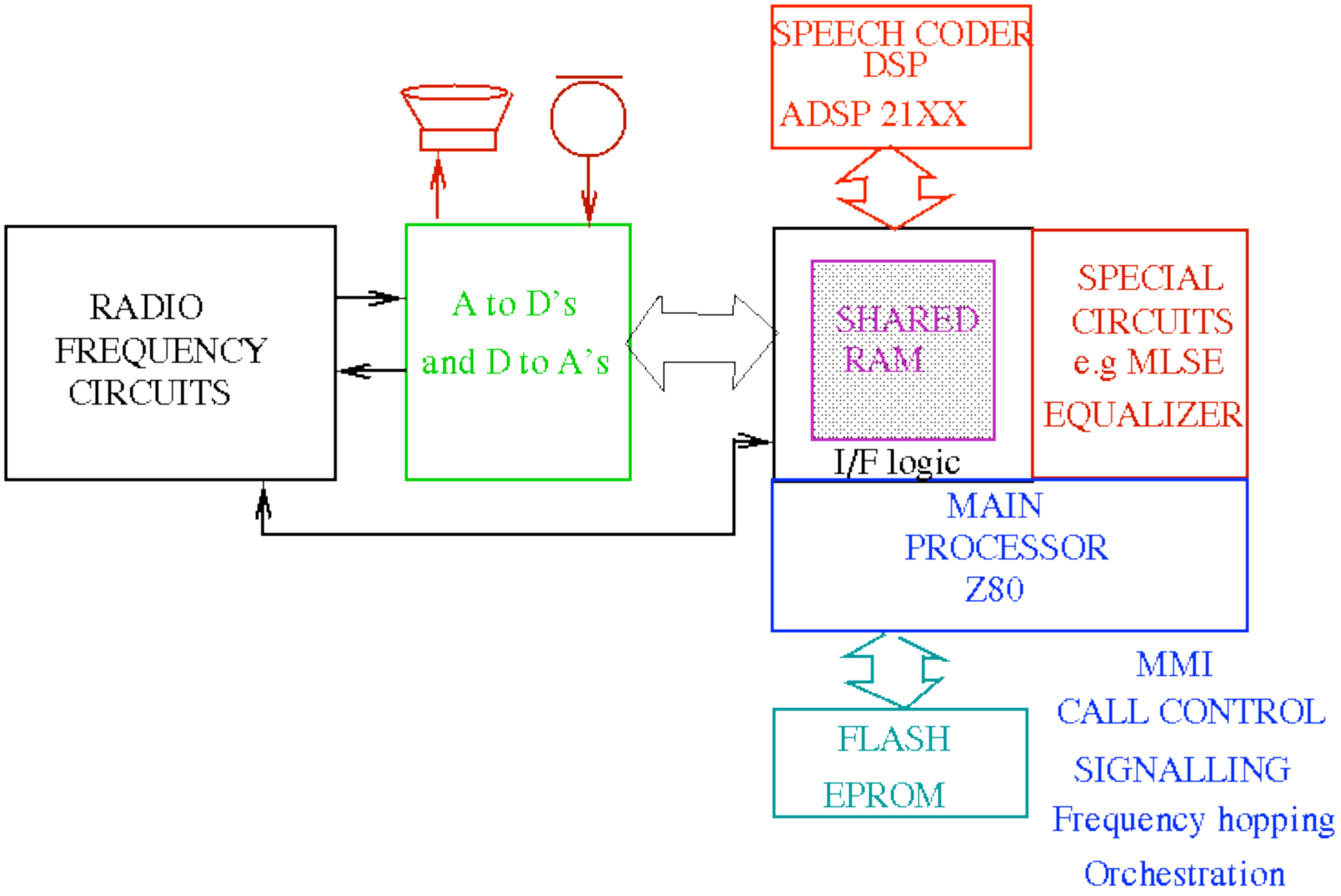
EMBEDDED PROCESSORS: -SHARING OUR WISH-LISTS

HISTORY

- Cellphones probably the single highest volume application for embedded processors
- Cellphone requirements typical of embedded applications
- Digital cellphones traceable to military radio developments of the 1970’s. First time the processor played a significant part in the communications protocol
- CMOS processors were hard to find then (RCA 1802, 80C51)
- Mid ’80s: Cold War thawed, expertise was switched to cellphones. Other CMOS processors emerged.
- Z80-> AVR-> ARM all non-mainstream initiatives!

FIRST GSM PHONE ARCHITECTURE (1987)



Embedded processors: What is the product?

- Already from first digital cellphone, the processor is part of a larger ASIC
- The "product" comprises:

  -An ASIC core: A netlist and timing database that has been verified at one or more chip fabrication houses;

  -Software support and development tools (assemblers, compilers, linkers, OS)

EMBEDDED PROCESSORS IN MOBILE WIRELESS DEVICES

Used for:

1.Signal processing (layer 1)

2.Protocol stacks (layer 2)

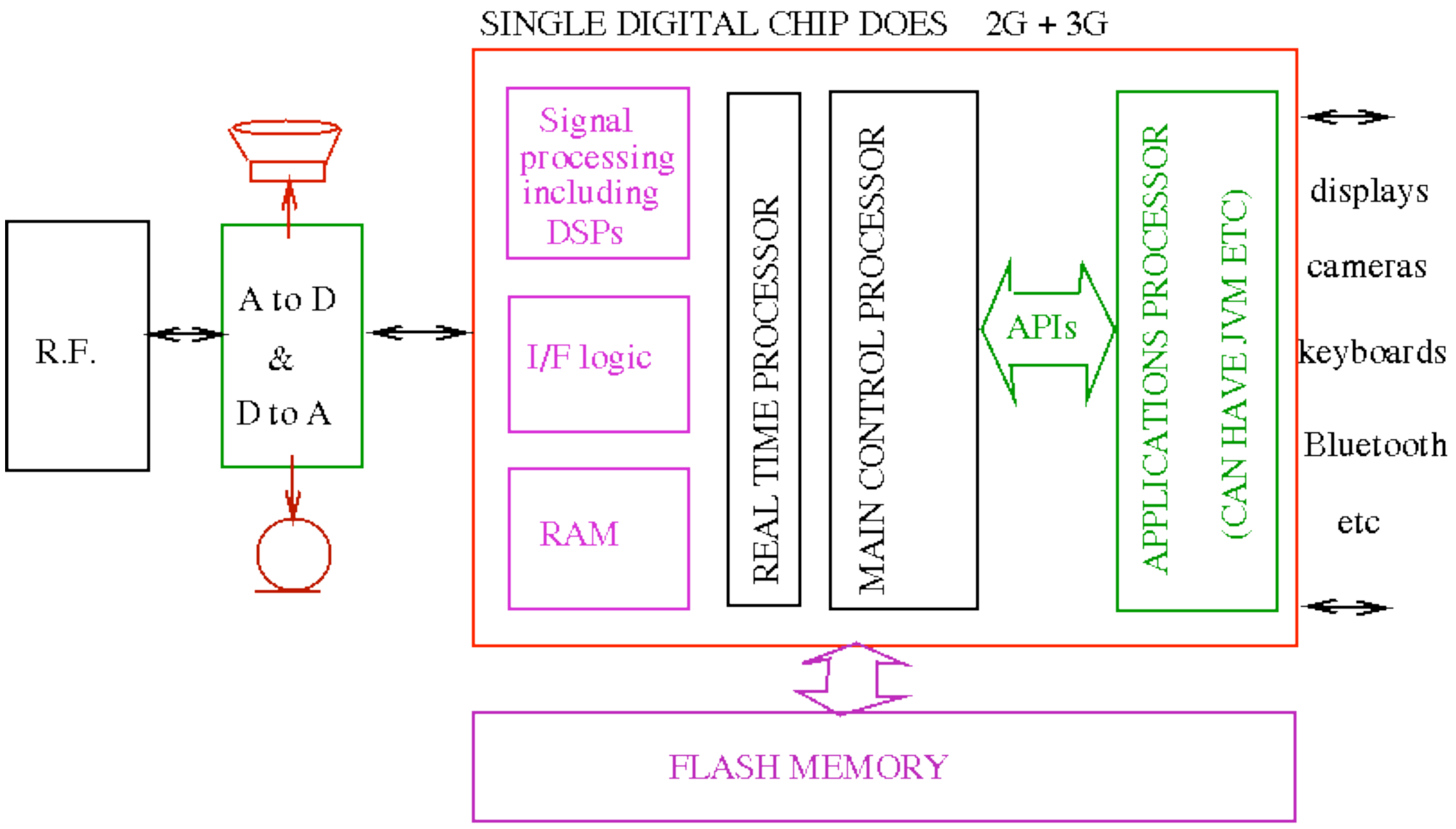
3.Signalling and control functions (layer 3)

4. Man-Machine interface
    - -Real-time orientated scheduler/Op-Sys

5. Vendor-supplied applications programs
    - -Dynamic allocation of RAM/stacks
    - -Fragment collection:-
    - -Hardware support? Speed penalty?

6. 3rd Party applications programs
    - -Security implications: Use separate processor

CURRENT DIGITAL PHONE ARCHITECTURES



WHERE DOES “EMBEDDED” DIFFER?

- Apart from speed/power, cost etc,

  Where are the real differences in the architectural features desired for “embedded” as opposed to more general purpose computing (e.g. PC)

GENERAL REQUIREMENTS

- For portable applications, low battery consumption is paramount (mA/MIP)
- Low-current sleep-modes
- Keep as many memory accesses as possible on-chip
- On-chip memory more costly than standard memory chips
- Contain pin-count explosion
- Memory 30% of system cost: No hard drive! Devise memory-efficient instruction sets
- Ease software development (Large, linear address space)
- Hard-logic accelerator assistance where appropriate. Viterbi, FFTs, log-arithmetic, long-arithmetic (public key)
- All Internet security issues (viruses, spoofing, keyloggers, identity theft etc)
- Non-modifiable core software (Hardware protection)

LOW POWER IS PARAMOUNT

...........................claims that it possesses a standby time of 540 hours and 9.9 hours of talk time. Its 55.9MB of integrated memory is more than..............

LOW CURRENT SLEEP MODE

- Processor should take zero current when idle

  -Lowest priority context executes a
  “stop clock to processor” instruction

  -OR of all interrupts re-applies clock

  -Use of static, CMOS logic seems to be implied
  but other processes could be mixed in.
  (current-mode bipolar more power efficient
  when working flat out?)

KEEP MEMORY ACCESSES ON CHIP

- Run programs in on-chip cache RAM
  (thank you for single-transistor static RAM)
- Can take perhaps 10 clock cycles to access external FLASH memory
  - -Don’t waste it: Do something else while waiting:-
    - -One-cycle context switch
    - -A register set per context (256 x 16 x 32)
    - -A small cache per context

CONTAIN THE PIN-COUNT EXPLOSION

- High probability that next external fetch address $A(n) = A(n-1) + L$
  - -Devise memory interface to have a "next" pin. Significant power reduction!
- Very high bitrate serial interface?
- Standard memory products are cheapest. Would such interfaces be interesting general standards?

PROGRAM MEMORY EFFICIENCY

-Memory typically 30% of cost and increasing

-Code compression/decompression techniques?

-Are 256 (one-byte instructions) not enough?

SO WHY NOT 1-BYTE INSTRUCTIONS?

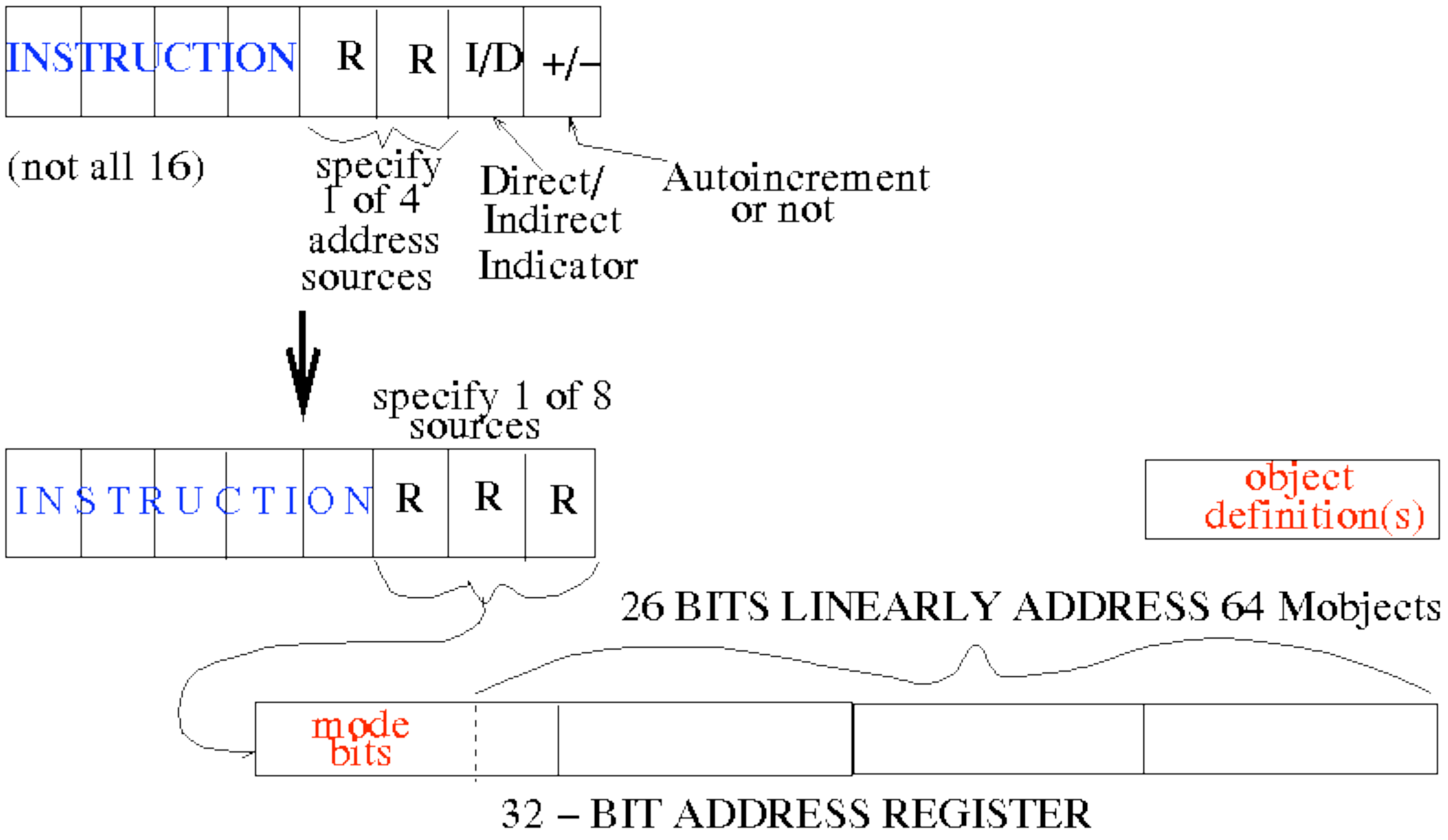
-Can have several specialized 1-byte instruction sets invoked routine-by-routine automatically upon CALL; e.g. Arithmetic; Logical; IO control

-Instruction words often loaded with other bits, e.g. addressing mode bits (Direct/Indirect; auto-increment; Immediate; base+displacement etc.)

Idea?: Relocate addressing mode bits to the address registers.

RELOCATION OF ADDRESSING MODE BITS

A typical memory–reference instruction:–



INSTRUCTION
R
R
I/D
+/–
(not all 16)
specify 1 of 4 address sources
Direct/ Indirect Indicator
Autoincrement or not
specify 1 of 8 sources
INSTRUCTION
R
R
R
object definition(s)
26 BITS LINEARLY ADDRESS 64 Mobjects
mode bits
32 – BIT ADDRESS REGISTER

Programmer-defined instruction sets (more than just "macros")

- Don't box-in the programmer's creativity

```
        ROUTINE: Funny_Function (argument_list)
        USE: My_Favorite_Instruction_Set
        TYPE: Matrix_of_Complex_Polynomials: A,B,C
Start:  Custom instruction 1
        Custom instruction 2
         -
         -
        RETURN
        END
```

EASE OF SOFTWARE DEVELOPMENT

- Program to be understood by others. To be understandable, programming language should be readable. To be readable, it must be pronounceable.
- Key characteristic of a “high-level” language is simple argument passing (always by address, never by value) and addressing of complex data structures
- Processor addressing hardware intrinsically maps directly to Language constructs (recursive address translation)
- Large, linear address space. ~64MByte=16MWords may be enough linearity for embedded processors.

  Non-linearity acceptable beyond that
- Variable size data types (requires dynamic memory allocation –hardware support if used often)

```
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    %2fS%3d1%2fJ%3d94DF54CB');
if(window.yzq_s)yzq_s();
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Hard-logic accelerators

- Public Key needs N-bit multiplication; N = 512–>2048.

- Fixed, systematic algorithms efficient in hardware (save on reading program):

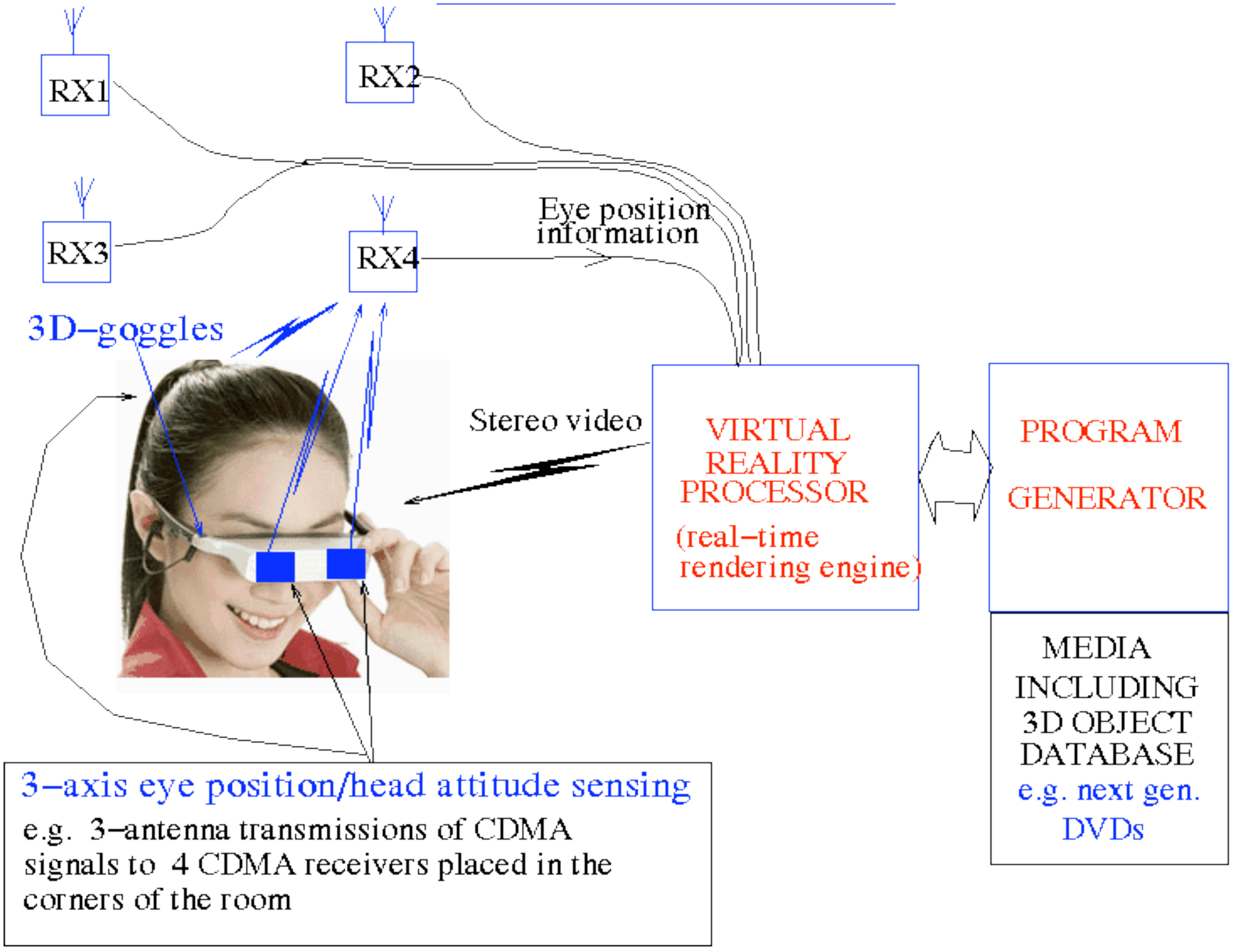
e.g. Viterbi MSLE for equalizers, error correction decoding
FFTs for future OFDM systems
FIR filters specified in standards

- Log- and complex-log arithmetic for signal processing and graphics rendering

THE FUTURE

- Voice, Email, Internet, TV, Radio, Music = “Multi-Media” on devices at home, in your car and in your pocket is a given.
- What would constitute a whole new industry?
- Virtual Reality is streets beyond 3D

VIRTUAL REALITY


RX1
RX2
RX3
RX4
3D–goggles
Eye position information
Stereo video
VIRTUAL REALITY PROCESSOR (real–time rendering engine)
PROGRAM GENERATOR
MEDIA INCLUDING 3D OBJECT DATABASE e.g. next gen. DVDs

3–axis eye position/head attitude sensing

e.g. 3–antenna transmissions of CDMA signals to 4 CDMA receivers placed in the corners of the room

CONCLUSIONS

- There are needs for processors with different design priorities than the PC
- They are not required as stand-alone chips, but are embedded in bigger chips
- What is the definition of an “embedded” processor?
- Is there concensus on what goes into the “wish-list”, or do we need a variety?