SoC Power Management Verification

Bhanu Kapoor (Mimasic), Shankar Hemmady (Synopsys), Kaushik Roy (Purdue)

We are at the crossroads of some fundamental changes that are taking place in the semiconductor industry. Power consumption has become one of the most important differentiating factors for semiconductor products due to a major shift in the market towards handheld consumer devices. Power is a primary design criterion for bulk of the semiconductor designs now. Power is a key reason behind the shift towards multi-core designs as increase in power consumption limits increases in clock speed at the rate we have seen in the past.

Voltage is the strongest handle for managing chip power consumption. Dynamic power is proportional to the square of supply voltage and leakage power has a linear relationship with it. In addition, leakage power has an exponential relationship with the threshold voltage of the device. This implies that if voltage can be controlled to optimally meet the performance then there can be much to be gained in terms of power savings.

This tutorial focuses on introducing fundamentals of the SoC power management design and verification to the attendees. We look in detail at some of key power management techniques that leverage voltage as a handle: Power Gating (PG), Power Gating with Retention (RPG), Multiple Supply Voltages (MSV), Dynamic Voltage Scaling (DVS), Adaptive Voltage Scaling (AVS), Multi-Threshold CMOS (MTCMOS), and Active Body Bias (ABB).

The use of above mentioned techniques imply certain power management architecture design and partitioning of design in terms of voltage islands that are controlled through power management signals. We look at the challenges in power management architecture design utilizing some examples that incorporate state-of-the-art power management techniques.

The use of above mentioned techniques also imply new challenges in validation of designs as new power states are created. We look into the characteristics of typical power states that exist in such designs and detail the techniques used in design validation. Techniques that leverage simulation, formal, and rule-based techniques are described in detail using examples. We make use of design examples from mobile baseband and application processor arena to aid explanation of these points.

Bhanu Kapoor

Bhanu Kapoor is a consultant and owner at Mimasic, a consulting services company in the area of low power chip design and verification. He has played leading technology development roles at EDA startups ArchPro (now Synopsys), Atrenta, and Verisity (now Cadence). He started his career with Texas Instruments where he played various technical roles (1987-99) at TI's R&D labs. He has helped set-up university technical advisory boards and played leading roles in joint industry and university research. Bhanu graduated from IIT Kanpur in 1987 with a degree in Electrical Engineering. He has received M.S. (1990) and Ph.D. (1994) degrees in Computer Science from SMU, Dallas. He is also an Adjunct Professor of Computer Science at SMU and serving as the Vice President of IIT Kanpur Alumni Association. He has authored over 30 IEEE/ACM conference/journal papers and has been granted 5 US patents in the area of low power design. Contact Information:

Bhanu Kapoor, 2701 Northridge Dr., Richardson TX 75082 USA | bkapoor@mimasic.com
| Cell Phone: +1-214-336-4973| http://www.linkedin.com/in/bhanukapoor

Shankar Hemmady

Shankar Hemmady is a Principal Engineer at Synopsys. He is responsible for verification solutions including planning, management, methodology and power-aware verification. Mr. Hemmady has designed, verified and tested, or managed the functional closure of over 25 commercial chips during the past 17 years of his tenure in the industry as an engineer, manager and consultant at 12 companies including AMD, Cirrus Logic, Fujitsu, Hewlett Packard, Intel, S3, Sun and Xerox. He has authored over 10 research papers and 10 articles in trade publications, and co-authored a book published by Springer, "Metric Driven Design Verification: An Engineer's and Executive's Guide to First Pass Success" in May 2007. Mr. Hemmady holds a B.S. in Electrical Engineering from the Indian Institute of Technology and an M.S. in Electrical & Computer Engineering from the University of Iowa. He completed Stanford's Advanced Management College executive program.

Shankar.Hemmady@synopsys.com

Kaushik Roy

Kaushik Roy joined the electrical and computer engineering faculty at Purdue University, West Lafayette, IN, in 1993, where he is currently a Professor and holds the Roscoe H. George Chair of Electrical & Computer Engineering. He was with the Semiconductor Process and Design Center of Texas Instruments, Dallas, where he worked on FPGA architecture development and low-power circuit design.

His research interests include VLSI design/CAD for nano-scale Silicon and non-Silicon technologies, low-power electronics for portable computing and wireless communications, VLSI testing and verification, and reconfigurable computing. Dr. Roy has published more than 400 papers in refereed journals and conferences, holds 8 patents, and is co-author of two books on Low Power CMOS VLSI Design (John Wiley & McGraw Hill). He is a fellow of the IEEE.

Kaushik Roy received B.Tech. degree in electronics and electrical communications engineering from the Indian Institute of Technology, Kharagpur, India, and Ph.D. degree from the electrical and computer engineering department of the University of Illinois at Urbana-Champaign in 1990.

kaushik@ecn.purdue.edu

Target Audience:

- Digital Design Engineers and Managers
- System Architects [Consumer handheld electronics, Wireless Networking]
- Verification engineers and managers for Wireless and Handheld Chips, GPS, Portable Music and Video Players, UWB, Bluetooth, Zigbee, and Wimax chips, Multi-core chip and systems
- EDA Tool Developers and Managers working on power tools
- Students and Professors pursuing research in the area of low power design

Pre-requisites:

- Basic Digital Design Knowledge, Verilog and VHDL Simulation
- Fundamentals of CMOS design and system design
- Power dissipation fundamentals are not required as it will be covered

Detailed Tutorial Program (Total Duration: 2:00 Hours)

- **Power Management Fundamentals** (**30 Minutes**)
  - System's perspective on power becoming a fundamental concern
  - Dynamic Power
  - Leakage Power and its impacts on 65nm & beyond
  - SoC Power Management Techniques
    - Clock Gating (CG)
    - Power Gating (PG)
    - Power Gating with Retention (RPG)
    - Multiple Supply Voltages (MSV)
    - Dynamic Voltage Scaling (DVS)
    - Adaptive Voltage Scaling (AVS)
    - Multi-Threshold CMOS (MTCMOS)
    - Active Body Bias (ABB)
  - Impact of Power Management Techniques on Dynamic and Leakage Power
- **Power Management Architecture Design Implications (45 Minutes)**
  - Power Gating and Retention Implications
  - Multi-voltage Implications
  - Power Management ICs (PMIC) Fundamentals
  - Design of Controller logic in conjunction with PMICs
    - Isolation, Retention, and Level-shifter Controls
  - Case Studies of Power Managed Designs
    - Renesas Processor
    - TI OMAP 2320
- **Power Management Architecture Verification Implications (45 Minutes)**
  - Design verification implications of each power management technique
  - Isolation, Retention, and Level-shifter verification
    - Simulation
    - Formal Techniques
    - Rule-based Techniques
  - Emerging power format standard [UPF and CPF efforts]
  - Case Studies for Verification
    - A 3-islands design with independent power on/off capabilities
    - Renesas Processor
    - TI OMAP 2320
    - Infineon Multimedia Enhanced Baseband Processor

Tutorial Summary:

SoC Power Management Verification

We are at the crossroads of some fundamental changes that are taking place in the semiconductor industry. Power consumption has become one of the most important differentiating factors for semiconductor products due to a major shift in the market towards handheld consumer devices. Power is a primary design criterion for bulk of the semiconductor designs now. Power is a key reason behind the shift towards multi-core designs as increase in power consumption limits increases in clock speed at the rate we have seen in the past. According to ITRS 2007 Report, power consumption is an urgent, short-term challenge, quickly shifting from a performance-driven active power crisis to a variability-driven leakage power crisis in the long term.

Voltage is the strongest handle for managing chip power consumption. Dynamic power is proportional to the square of supply voltage and leakage power has a linear relationship with it. In addition, leakage power has an exponential relationship with the threshold voltage of the device. This implies that if voltage can be controlled to optimally meet the performance then there can be much to be gained in terms of power savings. Figure 1 shows the power trends and growing importance of managing the leakage power especially the sub-threshold leakage component since use of technologies such as metal-gate can help mitigate gate-tunneling leakage component of leakage power.

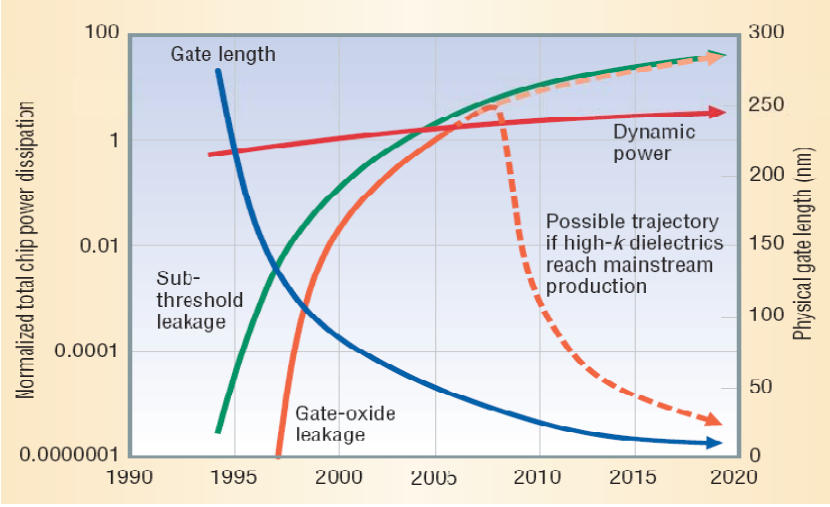

Figure1: Power trends and leakage power management (IEEE Computer 12/03)

In this tutorial, we look at some of the key SoC power management design techniques and their implications on design verification. These techniques include Power Gating (PG), Power Gating with

Retention (RPG), Multiple Supply Voltages (MSV), Dynamic Voltage Scaling (DVS), Adaptive Voltage Scaling (AVS), Multi-Threshold CMOS (MTCMOS), and Active Body Bias (ABB). The use of above mentioned techniques also imply new challenges in validation of designs as new power states are created.

Power Management Design Techniques

Voltage is the strongest handle for managing chip power consumption. The ability to use voltage as a system-level variable allows system-on-a-chip (SoC) designers to run different functions at different voltages and frequencies. Voltage islands have been used in use in some very high-volume commercial chips. These include cell phone ICs from companies like Texas Instruments and Freescale, general purpose processors from Intel and IBM, and chips that go in various handheld applications such MP3 players, video players, and GPS applications. Underlying the use of voltage islands are some of the voltage-based power management techniques that help reduce dynamic and leakage power. Figure 2 summarizes some of these power management techniques that make use of voltage as a handle. A brief description of each of the techniques follows next.

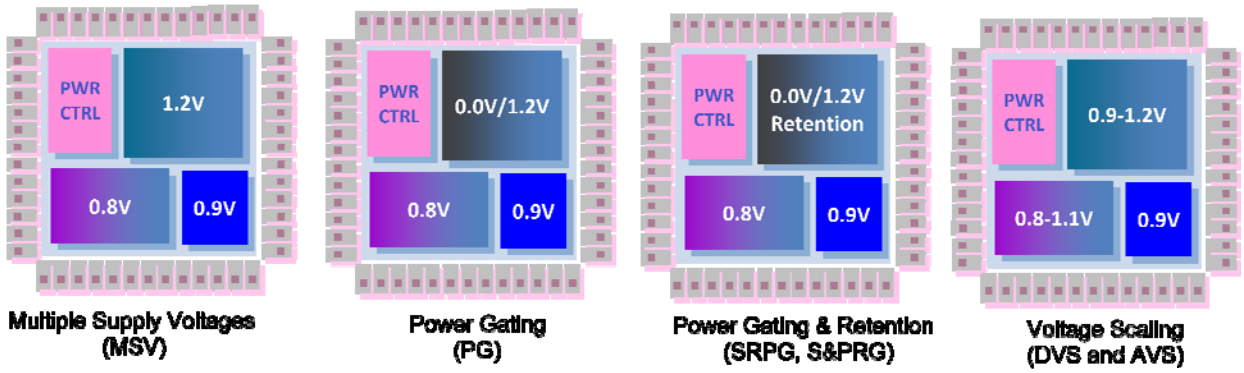

Figure 2: Summary of power management techniques that utilize voltage as a handle

Power Gating (PG)

Power gating (PG) is a technique for eliminating leakage power consumption of unused blocks in certain modes of chip operation. The power supply to the power gated block is cut off via the use of a power switch thus almost entirely eliminating leakage. The outputs of a block float as a result of power gating.

Power Gating with Retention (RPG)

Power gating is a time consuming process; power up and down process can take up a large number of clock cycle in high-speed applications. Power up is followed by a system reset. Resuming the operation, from the state where the system was prior to power down, requires the state of the system state to be stored and re-loaded upon power up.

State Retention Power Gating (SRPG)

A system stores its state in registers and memory blocks. The combinational logic present in between the registers provides a means for state propagation. In standby or idle mode, clock is gated and

registers simply save the state. Two power supplies, potentially derived from the same supply, are used to implement SRPG. There is a continuous power supply (Vddc) and a switchable supply (Vdd); state retention registers use both of these supplies where as the rest of logic is powered through Vdd and can be switched off.

Save and Restore Power Gating (S&RPG)

S&RPG is similar to SRPG in concept but differs significantly in implementation. The state of the system is moved to a memory array instead of saving them locally in the registers. Before entering the idle or standby mode, the states of the registers is captured and copied into a memory array.

Multiple Supply Voltages (MSV)

Different blocks of a chip can operate at different voltages based on performance requirements; voltage supplies can be always-on or turned off. Each partition associated is with a fixed operating voltage.

Level-shifters will be needed on signals that cross voltage boundaries. Timing may need to take into consideration multiple operating points when considering the paths that cross voltage domain boundaries. PG may be used along with MSV; both isolation and level-shifting may be required on some paths.

Dynamic Voltage Scaling (DVS)

Different applications that run on a processor may have varying performance requirements. These applications can be effectively run at different voltages in various modes of the chip operation.

Appropriate voltage can determined through a frequency-based voltage lookup table. PMIC can be directed by the power controller to provide the appropriate supply. Level-shifters are needed on signals that cross voltage boundaries. Level-shifters adapt to shifting from a scaled island scenario to a fixed voltage level or from a fixed voltage level to a scaled scenario. DVS is also known as dynamic voltage and frequency scaling (DVFS).

Adaptive Voltage Scaling (AVS)

From a power management concept standpoint, AVS is similar to DVS. However, unlike DVS which uses table lookup, AVS is closed loop system and power controller interfaces with a monitor in the scaled block to determine frequency needs and then directs the PMIC to provide appropriate voltage. Level-shifting needs are similar to that of a DVS scheme. Design and verification implications are similar to that of DVS scheme.

Multi-Threshold CMOS (MTCMOS)

Sub-threshold leakage increases exponentially with decreasing threshold voltage (Vth). The performance of the device is dependent upon different between the supply voltage and the Vth; lower Vth implies higher performance. A foundry will typically provide two or three libraries with different Vth's that can be effectively used to optimize leakage; in case of two Vths, lower Vth devices are used on the critical paths and higher Vth elsewhere.

Active Body Bias (ABB)

Active back bias (ABB) voltage, applied to wells of N-MOS and P-MOS transistors, is used to set the threshold voltages and leakage currents precisely in order to improve speed and at the same time control device sub-threshold leakage. The active back bias applies a voltage to the well of devices and this voltage can be generated by a PMIC.

If the leakage increases with age, temperature, or other conditions, changes in bias supply can be used to compensate. Compensation is required for process variations also; ABB is likely to become a necessity at 45nm and below.

Power Types Targeted and Design Verification Implications

Power management techniques mentioned in the previous section help address different components of power consumption. Dynamic and leakage power consumption is targeted by these techniques. Most of the portable consumer devices such as cell-phones spend majority of time in standby mode where mainly leakage power is consumed. In targeting leakage power, special attention is paid to both active and standby leakage power.

Figure 3 shows impact of each of these techniques of the above mentioned three key power types: Dynamic Power, Active Leakage Power, and Standby Leakage Power. The targets are standby leakage power, active leakage power, and dynamic power reduction. Green indicates primary effect and yellow indicates a secondary effect of the technique. White space indicates either little/no effect or an existence of an alternate method to have the same primary effect. For example, PG cuts off dynamic power too but clock gating can be used to have the same effect on dynamic power. But standby leakage remains an issue in presence of clock gating. A high-level impact on verification is also indicated. We will look into verification implications in detail next.

			Power Being Managed		
Technique			Standby Leakage	Active Leakage	Dynamic
Power Gating	PG				
Retention with PG	RPG				
Multiple Supply Voltages	MSV				
Dynamic Voltage Scaling	DVS				
Adaptive Voltage Scaling	AVS				
Multi-Threshold CMOS	MTCMOS				
Adaptive Body-Biasing	ABB				

Primary Secondary Verification Impact

Figure 3: Impact of various techniques on power types targeted and verification

Design verification in the context of power management techniques discussed in previous sections has some unique challenges. The design description languages at gate and higher level of abstraction don't have a notion of voltage as a variable. This was the first obvious gap that is now being addressed through the development of power formats such as UPF under the guidance of IEEE working group p1801.

The use these power management lead to some unique verification problems that did not exist before. Some example of these verification issues include:

- Isolation / Level Shifting Errors – Power domains should be isolated under powered down to avoid floating signals driving active regions and voltage domain crossings should be appropriately level shifted.
- Power Control Sequencing Errors – Voltage changes and power shutdowns are typically regulated in a sequence that must be adhered to by the design.
- Retention Sequencing/Selection Errors – If retention is being used in the context of power gating then one must ensure a proper selection of retention registers and signal sequencing the context of SRPG and S&RPG techniques.
- Hardware-Software Deadlocks – Power management is typically controlled by application through the software layer and incorrect power sequencing can lead to hardware-software deadlocks in the design.
- Power-on-reset / Bring-up problems – A large number of issues can result due to incorrect power-on-reset as design transitions through different power modes during the course of its operation.
- Power Connectivity – Now you have many voltage rails in the design and an incorrect connection of a net to a voltage rail will likely cause a design re-spin.

Addressing these and several other issues that arise due to the use of power management techniques require careful co-ordination in design verification plans utilizing simulation, formal, and rule-based verification techniques. Some of the key verification implications of power management are listed below:

- **Simulation:** Power management adds new power states to the design; verification plan must ensure existence of test scenarios to validate chip functionality in these states as well as sequencing among these states. Figure 4 shows growth in verification complexity due to increased number of power states in a typical consumer device that employs power management techniques mentioned in this article.

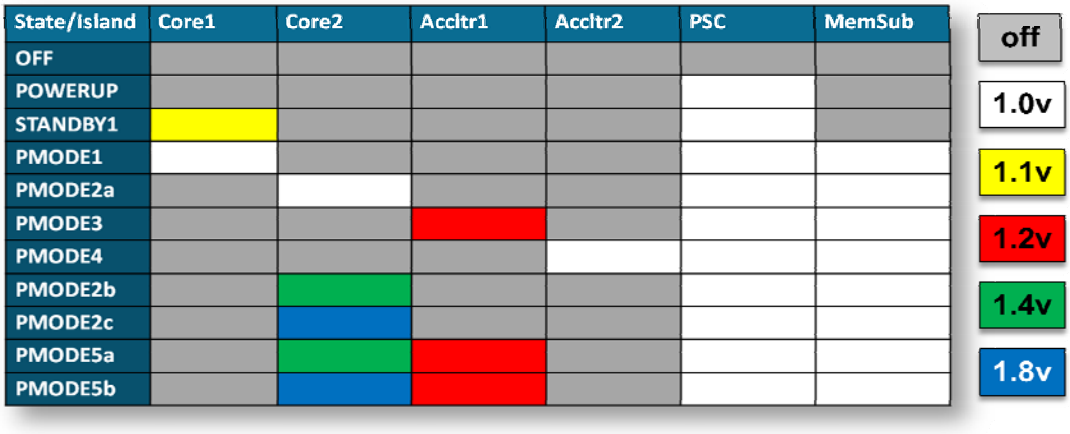

Figure 4: Power management techniques quickly add to verification complexity growth

- The use of power gated regions in the design requires proper isolation and isolation can be validated in the context of simulation-based verification plans. Typically, isolation can be used at the inputs or at the outputs or both at the inputs and outputs of the power-gated regions.
- Voltage changes are typically much longer events compared to clock cycles and ensuring clocks are gated during the voltage changes will help reduce power consumption during these changes. Monitoring signal activities during the course of simulation helps detect such issues.
- There are simulator feature implications here i.e., incorporate effects of voltage changes in the simulation engine. There are test-bench writing implications i.e., enhance test cases with the help of new simulator features along with the models of PMIC to validate the workings of the power controller.
- Power-on-rest issues will show up during the course of simulation only-if simulation infrastructure incorporates the effects of power gating in the design being simulated.

- **Formal:** Some power management features can also be validated using formal techniques; assertion-based as well as equivalency. Typically, there exist a set of formal relationships among power states and sequences that can be cast as assertion problems.

  As design goes through various levels of abstraction, equivalency of design looking from power architecture perspective can be established by a formal tool.

  Power management adds new elements to the design and these additions can be validated to be formally correct; a good feature for insertion tool also to guarantee correct-by-construction method.

  The behavior of assertions should be examined in the context of power gated designs. What happens to these assertions when a domain is powered off? Should these assertions be

suspended while the domain is powered off? Should these assertion be checked only once during the initial bring up?

- **Rule-Checking:** There are issues that don't fall in either the simulation or formal category and must be checked through a mechanism that also examines the structure of the design. A buffer introduced by synthesis can cause a re-spin but may look perfectly OK to the simulation and formal tools.

  There are situations which require always-on buffers to be placed on special signals in the context of power-gated designs and power-gated design that use retention. Ensuring correct instantiations of these always-on buffers is critical to correct functioning of the design.

  Power connectivity issues on the netlist with power and ground nets can be addressed via rule checking mechanisms that have the knowledge of power domains in the designs and associated supply nets. This will avoid issues such as isolation cells, level-shifters, and always-on buffers being connected to a switched supply.

Summary

Power consumption has become one of the most important differentiating factors for semiconductor products due to a major shift in the market towards handheld consumer devices. Power is a primary design criterion for bulk of the semiconductor designs now. Power is a key reason behind the shift towards multi-core designs as increase in power consumption limits increases in clock speed at the rate we have seen in the past. Voltage is the strongest handle for managing chip power consumption. We looked at some of the key SoC power management design techniques and their implications on the verification of overall design. Simulation, Formal, and Rule-Checking tools each a play important roles in power architecture validation at various levels of abstraction i.e., RTL, gate, and transistor-levels.

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