

2008 IEEE International Conference on Computer Design

October 12-15, 2008 Resort at Squaw Creek, Lake Tahoe, CA

Sponsored by:





IEEE Circuits and Systems Society



IEEE Catalog Number: CFP08ICD

ISBN: 978-1-4244-2658-4

ISSN: 1063-6404

© 2008 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE.

Table of Contents

Welcome	ix
Organizing Committee	xi
Program Committee and Reviewers	xii
Keynote Presentations	XV
Embedded Tutorial	xvi
Panel	xvi
Session 1.1 Fault and Error Tolerance (Logic and Circuits Track)	
Fault Tolerant Four-State Logic by Using Self-Healing Cells	1
Probabilistic Error Propagation in Logic Circuits Using the Boolean Difference Calculus	7
A Novel, Highly SEU Tolerant Digital Circuit Design Approach	14
Session 1.2 Tree Construction (EDA Track)	
Power-State-Aware Buffered Tree Construction	21
A Parallel Steiner Tree Heuristic for Macro Cell Routing	27
Configurable Rectilinear Steiner Tree Construction for SoC and Nano Technologies	34
Session 1.3 Formal Verification (Verification and Test Track)	
Improving SAT-Based Combinational Equivalence Checking Through Circuit Preprocessing Fabrício Vivas Andrade, Leandro M. Silva, Antônio O. Fernandes	40
Ant Colony Optimization Directed Program Abstraction for Software Bounded Model Checking	46
Propositional Approximations for Bounded Model Checking of Partial Circuit Designs	52
Session 2.1 Application-Specific Processing Elements (Processor Architecture Track)	
Energy-Precision Tradeoffs in Mobile Graphics Processing Units	60
Dynamically Reconfigurable Soft Output MIMO Detector	68

Applying Speculation Techniques to Implement Functional Units	74
Accelerating Search and Recognition with a TCAM Functional Unit	81
Improved Combined Binary/Decimal Fixed-Point Multipliers	87
Architecture Implementation of an Improved Decimal CORDIC Method	95
Session 2.2 Clock Distribution (EDA Track)	
A Study of Reliability Issues in Clock Distribution Networks	101
Temperature-Aware Clock Tree Synthesis Considering Spatiotemporal Hot Spot Correlations	107
Custom Rotary Clock Router	114
Safe Clocking Register Assignment in Datapath Synthesis	120
Gate Planning During Placement for Gated Clock Network	128
Session 2.2 Networks-on-Chip (Computer Systems Track)	
Near-Optimal Oblivious Routing on Three-Dimensional Mesh Networks	134
Design of Application-Specific 3D Networks-on-Chip Architectures	142
Mathematical Analysis of Buffer Sizing for Network-on-Chips under Multimedia Traffic	150
A Resource Efficient Content Inspection System for Next Generation Smart NICs	156
Contention-aware Application Mapping for Network-on-Chip Communication Architectures	164
Session 3.1 Circuit Design (Logic and Circuits Track)	
Area and Power-Delay Efficient State Retention Pulse-triggered Flip-flops with Scan and Reset Capabilities Kaijian Shi	170
Adaptive SRAM Memory for Low Power and High Yield	176

On-Chip High Performance Signaling using Passive Compensation	182
A Random and Pseudo-Gradient Approach for Analog Circuit Sizing with Non-Uniformly Discretized	
Parameters	188
Characterization and Design of Sequential Circuit Elements to Combat Soft Error	194
Comparative Analysis of NBTI Effects on Low Power and High Performance Flip-Flops	200
Session 3.2 SoC, Memory, and Analog Testing (Verfication and Test Track)	
In-Field NoC-Based SoC Testing with Distributed Test Vector Storage	206
Test-Access Mechanism Optimization for Core-Based Three-Dimensional SOCs	212
Characterization of Granularity and Redundancy for SRAMs for Optimal Yield-per-Area	219
Dynamic Test Scheduling for Analog Circuits for Improved Test Quality	227
Test Cost Minimization through Adaptive Test Development	234
Session 3.3 Application-Specific Systems (Computer Systems Track)	
Fine-grained Parallel Application Specific Computing for RNA Secondary Structure Prediction on FPGA Yong Dou, Fei Xia, Xingming Zhou, Xuejun Yang	240
A High-Performance Parallel CAVLC Encoder on a Fine-Grained Many-core System	248
Acceleration of a 3D Target Tracking Algorithm Using an Application Specific Instruction Set Processor Sébastien Fontaine, Sylvain Goyette, J.M. Pierre Langlois, Guy Bois	255
Seamless Sequence of Software Defined Radio Designs through Hardware Reconfigurability of FPGAs <i>Amir Hossein Gholamipour, Elaleh Bozorgzadeh, Lichun Bao</i>	260
Application Specific Instruction Set Processor Specialized for Block Motion Estimation	266
Prototyping a Hybrid Main Memory Using a Virtual Machine Monitor	272
Best Paper Session	
Computer Systems Track: Variation-Aware Thermal Characterization and Management of Multi-Core Architectures	280

Processor Architecture Track: Efficiency of Thread-Level Speculation in SMT and CMP Architectures — Performance, Power and Thermal	
PerspectivePerspective	286
Venkatesan Packirisamy, Yangchun Luo, Wei-Lung Hung, Antonia Zhai, Pen-Chung Yew, Tin-Fook Ngai	
Logic and Circuits Track: Analysis and Minimization of Practical Energy in 45nm Subthreshold Logic Circuits	294
EDA Track: Power-Aware Soft Error Hardening via Selective Voltage Scaling	301
Verification and Test Track: Reversi: Post-Silicon Validation System for Modern Microprocessors	307
Session 4.1 VLSI Signal Processing (Logic and Circuits Track)	
Digital Filter Synthesis Considering Multiple Adder Graphs for a Coefficient	315
A Family of Scalable FFT Architectures and an Implementation of 1024-Point Radix-2 FFT For Real-Time Communications	321
Optimization of Propagate Partial SAD and SAD Tree Motion Estimation Hardwired Engine for H.264 Zhenyu Liu, Satoshi Goto, Takeshi Ikenaga	328
Highly Reliable A/D Converter Using Analog Voting	334
Session 4.2 Simulation and Reliability (Verification and Test Track)	
Hierarchical Simulation-Based Verification of Anton, a Special-Purpose Parallel Machine J.P. Grossman, John K. Salmon, C. Richard Ho, Douglas J. Ierardi, Brian Towles, Brannon Batson, Jochen Spengler, Stanley C. Wang, Rolf Mueller, Michael Theobald, Cliff Young, Joseph Gagliardo, Martin M. Deneroff, Ron O. Dror, David E. Shaw	340
Post-Silicon Verification for Cache Coherence	348
Acquiring an Exhaustive, Continuous and Real-Time Trace from SoCs	356
CrashTest: A Fast High-Fidelity FPGA-Based Resiliency Analysis Framework	363
Session 4.3 Multi-threaded and Multi-core Architectures (Processor Architecture Track)	
Exploiting Spare Resources of In-order SMT Processors Executing Hard Real-time Threads	371
Quantitative Global Dataflow Analysis on Virtual Instruction Set Simulators for Hardware/Software Co-Design Carsten Gremzow	377

A Simple Latency Tolerant Processor	384
Low-Cost Open-Page Prefetch Scheduling in Chip Multiprocessors	390
Simulation Points for SPEC CPU 2006	397
Session 5.1 VLSI Arithmetic (Logic and Circuits Track)	
Synthesis of Parallel Prefix Adders Considering Switching Activities	404
Conversion Driven Design of Binary to Mixed Radix Circuits	410
Systematic Design of High-Radix Montgomery Multipliers for RSA Processors	416
An Improved Micro-Architecture for Function Approximation Using Piecewise Quadratic Interpolation	422
A Floating-Point Fused Dot-Product Unit	427
Session 5.2 Modeling, Estimation, and Simulation (EDA Track)	
Chip Level Thermal Profile Estimation Using On-chip Temperature Sensors	432
Early Stage FPGA Interconnect Leakage Power Estimation	438
Modeling and Analysis of Non-Rectangular Transistors Caused by Lithographic Distortions	444
A Macromodel Technique for VLSI Dynamic Simulation by Mapping Pre-characterized Transitions Dimitrios Bountas, George Stamoulis, Nestoras Evmorfopoulos	450
Pre-Si Estimation and Compensation of SRAM Layout Deficiencies to Achieve Target Performance and Yield Aditya Bansal, Rama N. Singh, Saibal Mukhopadhyay, Geng Han, Fook-Luen Heng, Ching-Te Chuang	457
Session 5.3 Multiprocessor and Multi-core Systems (Computer Systems Track)	
Frequency and Voltage Planning for Multi-Core Processors Under Thermal Constraints	463
Understanding Performance, Power and Energy Behavior in Asymmetric Processors	471
Optimizing Data Sharing and Address Translation for the Cell BE Heterogeneous Chip Multiprocessor	478
The 2D DBM: An Attractive Alternative to the Simple 2D Mesh Topology for On-chip Networks	486

Design and Evaluation of an Optical CPU-DRAM Interconnect	492
Session 6.1 Emerging Techniques (Computer Systems Track)	
Leveraging Speculative Architectures for Run-time Program Validation	498
Bridging the Gap between Nanomagnetic Devices and Circuits	506
Techniques for Increasing Effective Data Bandwidth	514
RMA: A Read Miss-Based Spin-Down Algorithm using an NV Cache	520
Combined Interpolation Architecture for Soft-decision Decoding of Reed-Solomon Codes	526
Session 6.2 Timing (EDA Track)	
Timing Analysis Considering IR Drop Waveforms in Power Gating Designs	532
A Dynamic Accuracy-Refinement Approach to Timing-Driven Technology Mapping	538
Modeling and Reduction of Complex Timing Constraints in High Performance Digital Circuits	544
SynECO: Incremental Technology Mapping with Constrained Placement and Fast Detail Routing for Predictable Timing Improvement	551
Is There Always Performance Overhead for Regular Fabric?	557
Session 6.3 Energy-Efficiency and Security in Processor Designs (Processor Architecture Track)	
Adaptive Techniques for Leakage Power Management in L2 Cache Peripheral Circuits	563
Energy-Aware Opcode Design	570
Making Register File Resistant to Power Analysis Attacks	577
Quantifying the Energy Efficiency of Coordinated Micro-Architectural Adaptation for Multimedia Workloads . Shrirang Yardi, Michael S. Hsiao	583
Suitable Cache Organizations for a Novel Biomedical Implant Processor	591

Issue System Protection Mechanisms	599
Session 7.1 Low Power (Logic and Circuits Track)	
Power Switch Characterization for Fine-Grained Dynamic Voltage Scaling	605
A Fine-Grain Dynamic Sleep Control Scheme in MIPS R3000	612
Run-time Active Leakage Reduction By Power Gating And Reverse Body Biasing: An Energy View	618
Energy-Delay Tradeoffs in 32-bit Static Shifters	626
Reliability-Aware Dynamic Voltage Scaling for Energy-Constrained Real-Time Embedded Systems	633
Session 7.2 Tools and Methodologies (EDA Track)	
Removing Hazards in Multi-Level Logic Optimization for Generalized Fundamental-Mode Asynchronous Circuits	640
Router and Cell Library Co-development for Improving Redundant Via Insertion at Pins	646
ECO-Map: Technology Remapping for Post-Mask ECO Using Simulated Annealing	652
Global Bus Route Optimization with Application to Microarchitectural Design Exploration	658
Fast Arbiters for On-Chip Network Switches	664
Session 7.3 Cache Architectures (Processor Architecture Track)	
Re-Examining Cache Replacement Policies	671
Two Dimensional Highly Associative Level-Two Cache Design	679
Exploiting Producer Patterns and L2 Cache for Timely Dependence-Based Prefetching	685
Ring Data Location Prediction Schemes for Non-Uniform Cache Architectures	693

ZZ-HVS: Zig-Zag Horizontal and Vertical Sleep Transistor Sharing to Reduce Leakage Power in On-Chip	
SRAM Peripheral Circuits	699
Houman Homayoun, Mohammad Makhzan, Alex Veidenbaum	
Author Index	707

Welcome to ICCD 2008!

On behalf of the Program Committee, we would like to welcome you to the 26th IEEE International Conference on Computer Design 2008! For a second time in a row the conference is being held in the quiet and inspiring mountainside of Lake Tahoe, California.

The International Conference on Computer Design (ICCD) encompasses a wide range of research and technical topics in the architecture, design, implementation, verification, and test of computer systems. Throughout its history, ICCD has retained its unique characteristics as the most diverse multidisciplinary venue for academic and industry practitioners to discuss practical and theoretical work in the field of computer design. As a tradition, ICCD is an international gathering of highly qualified researchers from industry and academia sharing ideas in whole daylong inspiring discussions.

The conference technical program consists of technical papers submitted to the Program Committee for evaluation and selected after a rigorous peer-review process, with an average of four reviews per paper. The technical papers are submitted to one of five conference tracks: Computer Systems Design and Applications; Processor Architecture; Logic and Circuit Design; Electronic Design Automation; and Verification and Test. The track committees are composed of world level technical experts in their disciplines, who review and select the best submissions. After the individual reviews are completed, each paper is discussed collectively by the track committee, to ensure equity and consistency in the selection process. The Program Chairs review the selections from the track committees and finalize the program.

ICCD is truly an international conference, with participation from researchers and developers from academic institutions, research laboratories, and industry design and development groups throughout the world. This year, the Program Committee received paper submissions from 33 different countries. More precisely the submissions came from: Australia, Belgium, Brazil, Canada, China, Denmark, Egypt, France, Germany, Greece, India, Iran, Israel, Italy, Japan, Lebanon, Netherlands, Norway, Pakistan, Poland, Portugal, Puerto Rico, Russia, Singapore, South Korea, Spain, Taiwan, Turkey, United Arab Emirates, United Kingdom, United States and Vietnam. Of the 306 papers submitted, the track committees accepted 106 papers (34% acceptance rate) for inclusion in the conference proceedings and for presentation at the conference. In addition, the conference program includes an embedded tutorial on the topic of "SOC" power management verification" organized by Bhanu Kapoor. Speakers, Shankar Hemmady, Prapanna Tiwari, Kaushik Roy and Manuel D.Abreu (from Synopsis, Purdue and SanDisk Corp.), will give their views on the subject. Furthermore, Sule Ozev and Reiner Hartenstein organized the conference panel that will address the question: "Will unaffordable von Neumann dominance enforce new directions in manycore architectures?"

The conference program features three keynote presentations from luminaries in our field: Fred Chong from University of California at Santa Barbara, Chris Rowen from Tensilica, and Christian Belady from Microsoft.

On behalf of the Organizing Committee, we would like to thank all 145 program committee members, and especially the track committee chairs, for their dedication and diligence in selecting an exceptional set of technical presentations. The investment of their time and insights is very much appreciated. Of course, ICCD would not happen without the excellent papers from the authors. Thanks to all of them as well!

On a personal note, we would like to thank our colleagues on the organizing committee for their efforts, their support, and their camaraderie. The efforts of Kevin Rudd, Past Chair; Kee Sup Kim, Finance Chair; Greg Byrd and Suleyman Sair, Publications Co-Chairs; Sule Ozev, Special Sessions Chair; Eren Kursun and Ben Juurlink, Publicity Chairs are all very much appreciated. In addition, we thank Bogdan Spinean, Catalin Ciobanu and Daniele Ludovici from TU Delft for migrating and maintaining the conference webpage and the overall technical support.

We are indebted to the support and guidance from the IEEE Circuit and Systems Society and the IEEE Computer Society as well as the IEEE Publications and Conference Management staffs.

The outstanding conference program at ICCD 2008 is a result of many individuals who contributed their time and expertise leading up to the event. The culmination of their efforts is the technical interchange, informal discussion, and personal communication that can only occur at the conference itself. In that regard, we hope you have a rewarding and enjoyable time at the conference. **Welcome to ICCD 2008!**

Carl Pixley General Chair

Peter-Michael Seidel Georgi Gaydadjiev Program Co-Chairs

Organizing Committee

General Chair Carl Pixley, Synopsys

Past General Chair Kevin Rudd, Intel

Program Chairs Peter-Michael Seidel, AMD

Georgi Gaydadjiev, TU Delft

Finance Chair Kee-Sup Kim, Intel

Publication Chairs Greg Byrd, NC State University

Suleyman Sair, Intel

Special Session Chair Sule Ozev, Arizona State University

Publicity Chairs Eren Kursun, IBM TJ Watson

Ben Juurlink, TU Delft

Web Site and Bogdan Spinean, TU Delft Catalin Ciobanu, TU Delft Catalin Ciobanu, TU Delft

Daniele Ludovici, TU Delft

Program Committee

Computer Systems Design and Applications Track

Valentina Salapura - Chair Fadi Kurdahi - Chair

Nader Bagherzadeh Matthias Blumrich Greg Byrd John Carter

Adrian Cristal Bronis de Supinski

Jim Holt

Michael Gschwind Bruce Jacob Manuel Jimenez Lizy Kurian John

Ben Juurlink David Kaeli Hyesoon Kim Kevin Leigh

Andreas Moshovos Hiroshi Nakamura Anthony Nguyen Hitoshi Oi

Timothy Pinkston Milos Prvulovic Amir Roth

Daniele Scarpazza Xiaowei Shen Yefim Shuf Dan Sorin

Vijayalakshmi Srinivasan

Karin Strauss Michela Taufer Pedro Trancoso Processor Architecture Track

John Glossner - Chair Jarmo Takala — Chair

Holger Blume Jim Bondi Bruno Bougard Mike Butler Ramon Canal Allen Cheng Henk Corporaal Brian Flachs Jose Fridman Roberto Giorgi Tony Jarvis Tor Jeremiassen Timothy Kam Stefanos Kaxiras Eren Kursun Hsien-Hsin Lee Mikko Lipasti Gabe Loh Trevor Mudge

Dionisios Pnevmatikatos Dmitry Ponomarev Miodrag Potkonjak

Emre Ozer

Peter Petrov

Jose Renau

Mike Schulte
Olli Silven
Balaram Sinharoy
Gary Tyson
Theo Ungerer
Mateo Valero
Alex Veidenbaum
Wayne Wolf
Chia-Lin Yang
Sami Yehia

Logic and Circuit Design Track

Vojin G. Oklobdzija - Chair Lars Svensson – Chair

Massimo Alioto
Bevan Baas
Kerry Bernstein
Ben Calhoun
Vikas Chandra
Marc Daumas
John Dielissen
Jo Ebergen
Henrik Eriksson
Guy Even
Dave Frank
Jie Gu

Masanori Hashimoto Nam Sung Kim Carl Lemonds William Li Nikola Nedovic Amy Novak Jelena Popovic Stefan Rusu Bogdan Staszewski

Andreas Steininger

Mile Stojcev

Nestoras Tzartzanis Kimivoshi Usami Nick van der Meijs Miroslav Velev Bart Zeydel Radu Zlatanovici Electronic Design Automation Track

Ryan Kastner - Chair Farzan Fallah – Chair

Anand Ragunathan Andy Pimentel Ankur Srivastava Azadeh Davoodi Bashir Al-Hashimi Bernard Courtois Chirayu Amin Deming Chen Dirk Stroobandt Eby Friedman Enrico Macii Huaizhi Wu Iris Bahar Janet Wang Jrg Henkel Serdar Tasiran Shih-Chieh Chang Shinji Kimura Soheil Ghiasi Taewhan Kim Xiaojian Yang Zhuo Li

Verification and Test Track

Patrick Girard - Chair Soene Tahar - Chair

Husam Abu-Haimed Davide Appello Dominique Borrione Alberto Bosio Luigi Carro Said Hamdioui Sybille Hellebrand Robert B Jones Thomas Kropf Tiziana Margaria Peter Maxwell Gordon Roberts Jun Sawada Klaus Schneider Xiaoyu Song Anna Slobodova

Mohammad Tehranipoor Erik Volkerink

Erik Volkerink Farn Wang Xiaoqing Wen

External Reviewers

Yuval Peress Rui Alves William Hung Rafael Arce-Nazario Pablo Ibanez-Maran Laurence Pierre Massimo Poncino Arash Arfaee Ali Irturk Joseph Babanezhad Renatas Jakushokas Zdravko Popovic Paolo Bennati Nebojsa Jankovic Lucian Prodan Bridget Benson Sumit Kumar Jha Nikola Puzovic Reinaldo Bergamaschi Zhanpeng Jin Wei Oin Letizia Bolzani Vaibhav Karkare Rodric Rabbah

Demid Borodin Michael Katelman Marco A Ramirez Salinas

Andrea Calimera Pertti Kellomaki Huan Ren

Jeremy Casas Faisal Khan Jonathan Rosenfeld

John Cavazos Changkyu Kim Paul Sack Frank Chen Daehvun Kim Emre Salman Yi-Zong Chen Minjang Kim Perttu Salmela **Dmitry Korchemny** Scott Chilstedt Kaushal Sanghai Selcuk Kose Josep M. Codina Oliverio J. Santana Mariane Comte Navda Santiago Sanjeev Kumar Tom Degryse Nagesh Lakshminarayana Ashoka Sathanur Martin Delvai Han-Lin Lee Ioannis Savidis

Giorgio Di Natale Victor Lee Asadollah Shahbahrami Luigi Dilillo Seung Lee Prassanna Sithambaram Karthik Duraisami Byeong Lee Ioannis Sourdis

Nur Engin Yue Li Radu Stefan
Hamed Fatemi Min Li Todor Stefanov
Felix Fernandez Chong-Shan Lin Bernhard Steffen
Markus Ferringer Chunchen Liu George Suarez
Goerschwin Fey ChunChen Liu Darao Suarez-Garcia

Ian Finlayson Anita Lungu Martin Swany Pierfrancesco Foglia Guojie Luo Mehdi Tahoori Gottfried Fuchs Darko Tasovac Pol Marchal Vishal Markandey Mihai Udrescu Matthias Fuegger Ty Garibay Hiroaki Matsutani Sascha Uhrig Peter Gavin Sally McKee Enrique Vallejo

Mike Gerdes Cor Meenderinck Guruprasadh Venkataramani

AmirHossein Gholamipour Waleed Meleis Javier Verda Mrinmoy Ghosh Gian Lorenzo Meocci Milena Vratonjic

Ruben Gonzalez Bart Mesman Muhammad Aqeel Wahlah

Isidro GonzA□ lezStefan MetzlaffChifeng WangVinodh GopalMiranda MiguelChengcheng WangDusan GrujicVeljko MihajlovicJohn-David Wellman

Meeta GuptaJarg MischeMark WohNissim HalabiHitoshi MizunumaJulian WolfMatin HashemiSeth MolloyChenyu YanAkira HatanakaKatell Morin-AlloryJung Sook YangSteve HinesDavid NovoChia-Hsiang Yang

Houman HomayounRogelio PalomeraBilal ZafarWen Hsiang HuDavid PapaAlenka ZajicChris HughesVassilis PapaefstathiouYimin ZhangDongkook ParkJi Zhang

Keynote Presentations

Towards More Sustainable Computer Design

Fred Chong, University of California at Santa Barbara



Fred Chong is the Director of Computer Engineering and a Professor of Computer Science at UCSB. He also directs the Greenscale effort in Energy-Efficient Computing, which involves over 20 multi-disciplinary faculty. Chong received his Ph.D. from MIT in 1996 and was a faculty member and Chancellor's fellow at UC Davis from 1997-2005. He is a recipient of the NSF CAREER award and his research interests include emerging technologies for computing, multicore and embedded architectures, computer security, and sustainable computing.

Green Computing: Big Challenges and Little SolutionsChris Rowen, Tensilica



Chris Rowen, Ph.D.is Founder, Chief Technology Officer, member of the board of directors, and Tensilica's first president. He was a pioneer in the development of RISC architecture at Stanford in the early 80s and helped start MIPS Computer Systems Inc. in 1984, where he served as Vice President for Microprocessor Development. Most recently, he was Vice President and General Manager of the Design Reuse Group of Synopsys Incorporated. He received a B.A. in physics from Harvard University and M.S. and Ph.D. in electrical engineering from Stanford University.

Lean IT: Lead or DieChristian Belady, Microsoft



Christian Belady is Microsoft's Principal Power and Cooling Architect for Global Foundation Services where his role is to improve both efficiency and cost in their online services infrastructure. In addition, his responsibilities included driving initiatives for sustainability in the data center and infrastructure space. Prior to joining Microsoft, Christian was a Distinguished Technologist for HP where his responsibilities included driving the technology direction in HP's server products and their environments as well as driving industry data center initiatives. In addition, his earlier employers include; Convex Computers (acquired by HP), TI and IBM. With over 60 US patents, Christian is an ASME Fellow, an IMAPS Fellow and a founding member of ASHRAE's TC9.9, which is responsible for developing data center guidelines. He was one of the early architects of the Green Grid, and continues to participate actively with the group. Christian has engineering degrees from Cornell University (BS) and Rensselaer Polytechnic Institute (MS) and a business degree from the University of Texas at Dallas (MA).

Embedded Tutorial

SoC Power Management Verification

Bhanu Kapoor, Mimasic Shankar Hemmady, Synopsys Kaushik Roy, Purdue University TBD, nVIDIA

Panel Session

Reset Microprocessor Hardware and Software Roadmaps for the Next 30 Years?

Moderated by:

Georgi Gaydadjiev, TU Delft

Panelists:

Tom Conte, Georgia Institute of Technology Ed Grochowski, Intel Corporation Joerg Henkel, University of Karlsruhe

Organized by:

Reinter Hartenstein, Kaiserslautern University of Technology Sule Ozev, Arizona State University