A Study of Reliability Issues in Clock Distribution Networks

Aida Todri  
UCSB, ECE Department  
atodri@ece.ucsb.edu

Malgorzata Marek-Sadowska  
UCSB, ECE Department  
mms@ece.ucsb.edu

Abstract - In this paper, we present a reliability study of clock mesh distribution networks. We analyze the electromigration (EM) phenomena and demonstrate their occurrence in clock mesh networks (CMN). Due to shrinking feature sizes in more advanced technologies, EM is becoming a more prominent reliability issue. Process variation, power supply noise, and clock gating are some of the factors that can increase electromigration in the clock mesh. We identify the potential EM branches by investigating current flows under various conditions. Our study shows that a clock mesh optimized for certain configurations of clock sinks may experience electromigration due to asymmetrical bidirectional currents flowing in some grid segments.

I. INTRODUCTION

Electromigration (EM) is the process of metal-ion migration due to high current density stress in metal and it has been studied extensively [2]. It causes the migration of metal ions that may result in metal buildup or depletion. The buildup of excessive metal produces hillocks that can create shorts between wires, whereas excessive metal depletion can change the wires’ resistivity.

A metal wire can experience electromigration failure if the dc current flowing though it exceeds the allowed density. EM susceptibility is higher on metal lines that have dc unidirectional current flows, such as power and ground lines. These lines are particularly susceptible to electromigration damage because they carry high density unidirectional dc currents. Signal lines carry dc pulsating bidirectional currents [5], which have less severe electromigration due to a self-healing process that is the result of the nullification of metal-ions migrating in each direction [5]. In the past, electromigration has been considered only in the context of power and ground supply networks. More recently, it has been also investigated in signal wires as well.

In 1989, Maiz investigated the symmetrical and asymmetrical bidirectional currents with various current density stresses and found that asymmetrical bidirectional currents can cause electromigration in metal wires and result in resistivity changes [6].

The currents flowing in a clock mesh are dc pulsating bidirectional currents. Because clock mesh networks are highly symmetric structures, it has been widely believed that they do not experience electromigration effects due to the symmetric nature of the flowing currents. In this paper we demonstrate that the currents flowing in a clock mesh are not all symmetric. Asymmetry may cause metal-ion migration to be dominant in one direction, which may lead to potential electromigration effects.

Designing clock distribution networks has become an increasingly challenging problem for deep submicron technologies. Clock networks have traditionally been designed as tree structures since these are easier to optimize. Mesh networks are also widely used to distribute the clock signal in high-performance microprocessors [1]. They achieve very low skew and jitter, but consume more power than clock trees. With technology scaling and tight power budgets, the clock networks are designed to provide nearly zero skew for low power budget. Such constraints prompt engineers to design clock networks with stringent geometries. In this work, we study the current flow in clock mesh networks and demonstrate the existence of asymmetric bidirectional currents. This asymmetry is amplified by process variations, power supply noise, and clock gating. Figures 1a and 1b depict the clock distribution networks discussed in this paper. An empirical model for electromigration was developed by J.R. Black. He gave a formula to estimate the mean time to failure (MTTF) of a wire taking electromigration into account [3]:

\[
MTTF = \frac{C}{J^n} \exp\left(\frac{E_a}{kT}\right)
\]

where \(C\) and \(n\) are empirical constants, \(J\) is the current density, \(E_a\) is the activation energy for the electromigra-
tion mechanism, $k$ is the Boltzmann constant, and $T$ is the temperature [3]. Thus, the effects of electromigration can be computed when the dc current stresses on the branches of a clock mesh are known. In addition, a large amount of current can generate significant heat (self-heating) due to the wires’ resistivity. This phenomenon, called Joule heating, accelerates to EM failure mechanism. Chang et al [14] describe the combined mechanisms of electromigration and self-heating. According to them, due the EM stressing, the cross-sectional area of a wire is reduced and the local current density increases. The material left behind can be so thin that the high current density induces Joule heating and raises the local temperature. This further shortens the MTTF and a wire segment may even melt and partially vaporize the remaining metal. In this study we consider the combined effect of electromigration and Joule heating.

The remainder of this paper is organized as follows. In Section II we introduce the design and architecture of clock networks with mesh structure. In Section III, we briefly discuss the asymmetrical bidirectional currents. In Section IV, we analyze EM and Joule heating for various conditions. In Section V, we discuss our experiments and conclude in Section VI.

II. CLOCK MESH NETWORKS

The global clock distribution is designed to have the minimum skew among all registers (clock sinks). For high-performance microprocessors, clock distribution networks are often designed as a tree that drives a single grid.

Tree networks have low latency, low power, minimal wiring track usage, and low skew. However, without the grid, trees must often be rerouted when the location of clock pins change or when the load capacitances change significantly [1]. A clock mesh provides a constant structure so that the tree and mesh it is driving can be designed early to distribute the clock signal close to every location where it may be needed. The mesh reduces local skew by connecting nearby points directly and creating redundant paths.

There are various structures of clock mesh networks. The mesh only structure consists of a uniform mesh driven by a global tree, shown also in Figure 1a. The clock sinks (flip-flops) are directly connected to the nearest mesh branches. The hybrid clock mesh structure is a combination of a clock mesh and various local trees. The trees distribute the clock signal from the mesh to the flip-flops in the regions, shown also in Figure 1b [9].

The clock tree driving the mesh can be designed as an H-tree [9] or an asymmetric tree with clock buffers of various sizes [11]. We will discuss both scenarios and their impact on electromigration and Joule heating. Similarly, clock sinks can be designed such that all are identical. However, non-uniform sinks are common in most designs [10]. In our study, we perform reliability analysis on both uniform and nonuniform sink configurations.

The clock mesh is designed as a regular grid of a size $m \times n$ where $m$ is the number of row tracks and $n$ is the number of column tracks. In this study, we assume that the clock network is optimized for zero skew and minimum area similar to those described in [9]. Minimum area is crucial to achieve low power consumption given that the clock network is large and covers the whole chip. Overdesigning the clock network to eliminate its susceptibility to electromigration by decreasing current density significantly increases power consumption. For 30% of an over-designed area of a clock mesh we may have an increase in clock power consumption of up to 53%.

III. ASYMMETRIC BIDIRECTIONAL CURRENTS

Bidirectional currents flow in both directions during the clock period. The currents flowing in the clock mesh are bidirectional. The clock’s rise and fall transitions are charging and discharging events for its sinks.

Asymmetric bidirectional currents have non-equal amounts of current flowing in the opposite directions. In the next section we will demonstrate that indeed such asymmetric bidirectional currents exist in a clock mesh and are caused by the different paths that currents take for charging and discharging the clock sinks. Figure 2 shows the waveforms of bidirectional currents for symmetric and asymmetric conditions.

The amount of current for each direction can be obtained by performing a time domain simulation of a transition and integrating the current through the branch over the simulation time, as:

$$I_{\text{dc}} = \frac{1}{T} \int_{0}^{T} i(t) dt$$

where $T$ is the clock period, $i(t)$ is the time varying current, and $I_{\text{dc}}$ represents the positive and negative direction flowing currents for the rise and fall transitions. We define the degree of asymmetry, $A$, as the ratio of currents flowing in the opposite directions as:

$$A = \frac{I_{\text{dc}}}{I_{\text{dc}}}$$

Asymmetric currents with densities greater than the allowed amount can lead to electromigration reliability issues because such currents will induce more metal-ion
migration in one direction that over time will degrade the wire.

IV. THE EM AND JOULE HEATING ANALYSIS

In this section we analyze various conditions in which electromigration occurs. Clock meshes are often designed to have nearly zero skew among the registers while having non-uniform clock drivers and/or loads. In the following subsections, we show that under such conditions it is possible to have asymmetric bidirectional currents. Additionally, we demonstrate the increase in bidirectional currents under various conditions such as process variations, power supply noise, and clock gating.

A. Clock driver sizes

In an optimized clock network with a regular grid, uniform sinks and buffers, the current flow in the mesh is bidirectional and symmetric with current waveforms similar to that shown in Figure 2a. The amount of current for charging and discharging transitions are both the same. For such clock networks, the branches of the clock mesh have average currents $I_{dc}$ close to zero and are not susceptible to electromigration. Under such conditions self-healing occurs because the metal-ion migration effects for each direction nullify each other.

However, depending on the functionality and timing constraints, clock drivers (clock tree buffers) can be non-uniform and still maintain the skew constraints between the registers [11]. To investigate the current flow in an optimized clock network with a regular clock mesh and uniform clock sinks, but non-uniform clock buffers, we consider a sample clock network, as shown in Figure 3. It is a 4x4 mesh with two drivers and one sink. We consider two cases. In the first optimized clock network, the buffers of the clock mesh are of sizes $X_1$ and $X_2$ and in the second clock network, the buffers are of sizes $X_1$ and $X_3$. The clock sink capacitance values are set to 35pF, which are consistent with real designs [1].

The non-uniform size buffers have different charging and discharging capabilities that create asymmetric bidirectional currents on the clock mesh. One of the drivers is dominant during the charging stage of the clock cycle and the other driver is dominant at discharging. Figure 4 shows the current flows for uneven buffer sizes.

\[
\begin{align*}
\text{Driver} & \quad \text{Clock Grid} \\
& \quad \text{Sink} \\
\end{align*}
\]

Fig. 3. The dominant charging and discharging currents for different size drivers.

In Figure 5a we show the waveforms of asymmetric bidirectional currents as a function of driver sizes. In Figure 5b, we show the asymmetry ratio also as a function of driver sizes.

\[
\begin{align*}
\text{Fig. 5. Bidirectional current waveform, (a) symmetric and (b) asymmetric.}
\end{align*}
\]

Even though the average current $I_{dc} = I_{pdc} - I_{nnc}$ flowing in an optimized clock network with non-uniform drivers is within allowed margins for symmetric bidirectional flow, the amount of current flowing on each direction is not symmetric, with $I_{pdc} > I_{nnc}$ or $I_{nnc} < I_{pdc}$. Such current flow asymmetry allows more metal-ion migration to occur in one direction, which over time can lead to wire failure. Li et al [13] reported that in some cases a 38% change in current density can shorten the mean time to failure, $MTTF$, by a factor of 26.

From this experiment, we observe that in a clock mesh not all bidirectional currents are symmetric and varying buffer sizes introduce asymmetric bidirectional current flow on the clock mesh. The asymmetry ratio linearly increases with the non-uniformity of driver sizes.

B. Process variations

Process variations are characterized as temporal and spatial effects [12]. Temporal variations are typically related to circuit activity. Spatial variations are manufacturing dependent and demonstrate themselves as either variances of geometric dimensions of wires, or parameter variations. Here, we consider the geometric variations of the clock mesh tracks and variations of clock drivers’ and sinks’ widths. We represent the variations in the transistor’s width, length, and threshold voltages as the varia-
tions of the clock driver/sink sizes. The variation of the clock mesh track widths are modeled as changes of the parasitics’ impedance of the tracks. The local interconnects connect the clock inputs of the flip-flops directly to the nearest point on the clock mesh. The loading on the clock mesh can differ due to the process variations that affect the flip-flops and local interconnects. We represent the flip-flops and local interconnects’ parasitics as capacitors, similar to [11]. Process variations of clock sinks are represented as changes in the capacitor size. The ranges for all parameter variations are within 10 to 20% of their nominal values [12].

Figure 6 shows the maximum absolute value of a difference between charging and discharging currents on a branch for which \( I_{dc} > I_{max} \) or \( I_{dc} > I_{max} \). \( I_{max} \) is the maximum allowed current on a branch. These currents are obtained as function of track width percentage change, clock sinks’ size change and clock driver strength variations.

For some branches, the current flow increases up to 48.6% as a function of process variations, clock driver and sinks’ sizes, and clock mesh widths. In some branches, the current flow increases and surpasses the allowed amount. Additionally, process variations can induce asymmetric bidirectional current flows with ratios up to 1.25. Figure 7 shows the asymmetry ratio of the current flows as a function of track width variations.

Even though under process variation the clock mesh networks provide more skew stability than clock trees, they may experience reliability issues in the clock mesh branches due to asymmetric current flow. Such a phenomenon has not been considered during the design of the clock mesh and neglecting it may lead to significant reliability issues.

C. Power supply noise

Power supply noise can significantly impact the performance of a circuit by increasing the delay. It can also impact the charging and discharging effectiveness of clock drivers, which can cause changes in the current flow on the clock mesh. Figure 8 shows these phenomena.

For some branches on the clock mesh, there will be asymmetric current flowing due to the imbalance of the charging and discharging currents provided by driver \( A \). We apply power supply noise to one of the clock drivers and measure its impact on the charging and discharging current. Initially, we apply the power supply noise to uniform size clock drivers, clock sinks, and mesh track widths. Next, we apply power supply noise and process variations on the clock mesh, clock drivers, and sinks. Figure 9a shows the amount of current flow as a function of the power supply noise with uniform parameters. From this figure, we observe that the asymmetry ratio between charging and discharging currents increases when the noise and the degree of parameter variations increase. We
perform the experiment with non-uniform parameters while varying the amount of power supply noise applied to one of the clock drivers. Figure 9b shows the charging and discharging currents and 9c shows the asymmetry ratio. The asymmetry ratio with non-uniform parameters can reach up to 1.6 for 18% of induced power supply noise. The peak current can increase up to 9.4% from the allowed maximum current. Asymmetric bidirectional and peak currents can lead to electromigration effects.

D. Clock gating

Clock gating is a widely-used technique for reducing the dynamic clock power. Clock gating disables the clock signal to the idle parts of the circuit, thus avoiding power dissipation due to unnecessary charging and discharging of the unused circuit. Clock gating can be applied in either a fine- or coarse-grained manner. Hybrid clock structures can be gated by disabling any of the clock trees connected to the mesh.

Fig. 10. Clock mesh with clock-gateable tree.

We investigate the gated hybrid clock networks as illustrated in Figure 10. We apply clock gating on hybrid clock mesh networks with uniform and non-uniform parameters. Figure 11 shows the current flow after power gating is applied for both uniform and non-uniform parameters as a function of power supply noise on one of the clock drivers.

We observe that clock gating can introduce asymmetric bidirectional currents in structures with non-uniform parameters, even with no power supply noise. This is shown in Figure 11b. The ratio of asymmetry increases with power supply noise increase and in our experiments it reaches up to 1.58 for non-uniform parameters.

E. Mesh reduction (branch removal)

Clock mesh networks offer high tolerance to skew variation due to the many redundant branches [11] that provide a variety of paths for the current flow. However, some works consider removing some of the branches to reduce the clock mesh. This allows designers to trade-off clock skew and power dissipation. A reduced mesh retains only those branches that are critical to maintain the skew within certain margins. Normally, in the process of mesh reduction, we are concerned only with the effects on skew. Clock mesh branch removal may lead to electromigration by creating asymmetrical bidirectional currents.

Fig. 11. Current flow after clock gating as a function of power supply noise for (a) uniform and (b) non-uniform parameters.

Fig. 12. Current flow before and after mesh reduction.

To demonstrate this, we apply the mesh branch removal on an optimized clock network with uniform and non-uniform parameters. A sample setup is shown in Figure 12. We notice that removing some of the branches affects the current flow on the clock mesh and creates asymmetric bidirectional current flows and/or large peak currents. These become more dominant with increases in process variation and power supply noise. In the table in Figure 12, we show the current flows before and after mesh reduction. The asymmetry ratio increases with mesh reduction and it can reach up to 1.33.
V. EXPERIMENTS

We performed various experiments to observe the asymmetric bidirectional currents as functions of clock grid granularity and a percentage of the track widths overdesign. We considered up to 50x50 clock mesh granularities track widths that were overdesigned by up to 30%. The overdesigned track widths lower the current densities in the clock grid wires. Figure 13a shows the relationship between the \( MTTF \) and the percentage of overdesigned track widths. We notice that making tracks wider increases the lifetime of the clock mesh. The 30% wire width increase improves the MTTF by up to 30%. In Figure 13b, we show the power consumption as a function of overdesigned track widths. Power consumption increases with track widths’ increase and for the 30% wire width increase can reach up to 53%. Hence, blindly over designing the clock mesh by making the tracks wider can reduce the electromigration effect, but at the cost of a large increase in the clock’s power consumption.

Additionally, we computed the relationship between the \( MTTF \) and the asymmetry ratio of bidirectional currents. This is shown in Figure 13c. We observe that the increase in asymmetric bidirectional currents drastically reduces the lifetime of the clock mesh. Such an observation can be crucial in the initial stages of designing the clock mesh network, the clock buffer placement, and their sizing.

VI. CONCLUSIONS

In this paper, we have analyzed the clock mesh networks and their bidirectional currents. Our findings may seem counterintuitive as it is widely believed that the clock mesh currents are bidirectional but symmetric due to the symmetry of the grid. We demonstrated the existence of asymmetric bidirectional currents in clock networks which in modern designs are also designed to meet the power specifications. Asymmetrical bidirectional currents can lead to potential electromigration failures due to excessive metal-ion migration in one direction. Additionally, we showed that asymmetric bidirectional currents can occur under various conditions such as process variations, power supply noise, clock gating, and non-uniform clock drivers. Although over designing the clock mesh can reduce the electromigration/Joule heating, this comes at the cost of a very significant increase in power consumption. We believe that our observations will be helpful in designing robust and reliable clock mesh networks.

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VII. REFERENCES


Fig. 13. Results of various clock mesh granularities: (a) MTTF vs. percentage of track width overdesign, (b) power consumption vs. percentage of track width overdesign, and (c) MTTF vs. asymmetric ratio of bidirectional currents.