Temperature-Aware Clock Tree Synthesis Considering Spatiotemporal Hot Spot Correlations

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ABSTRACT

Temperature variation in microprocessors is a workload dependent problem. In such a design, the clock skew should be minimized with respect to temperature variation. Existing work has studied clock tree embedding perturbation considering time variant temperature variation. There is no existing method that can reduce skew variation. This paper develops an efficient yet effective simultaneous hotspot avoid embedding and thermal aware routing (TMST) method, where hotspot embedding avoid tree topology located in area with high temperature possibility and thermal aware routing reduce skew in tree path with more smooth temperature area. With a thermally tolerable tree structure, our method can reduce not only delay skew but also skew variation (skew violation range). Compared with existing temperature-aware clock tree method, our TMST solution reduces skew variation by 2X compared with the Greedy-DME (GDME) method of Edahiro and existing thermal aware clock synthesis TACO and PECO. With the scale from 100 down to 1 temperature maps, our TMST also guarantees the smallest wire length overflow. TMST reduces the worst case skew up to 4X than PECO and 5X than TACO.

I. INTRODUCTION

Clock synthesis has been extensively studied. Given a set of sinks (flip-flops), clock synthesis finds an abstract topology, embedding and minimizes mismatch of arrival times (i.e., skew) between sinks. Wire length minimizations under zero or bounded skew constraint were presented in [1], [2], [4]. However, process, supply voltage, and temperature variation induced skews were not considered. The exponential advance of very large scale integration (VLSI) technology has resulted in a high and non-uniform power dissipation over chips [4], which leads to a temperature gradient, i.e., spatial temperature variation over a chip that can cause non-negligible delay differences in both interconnects and devices. As clock signals are globally routed over chip, the temperature gradient can bring significant skew variations [5]. Therefore, the traditional constant zero/bounded skew routing methods become invalid.

The history of clock tree synthesis under thermal variation is short. TACO [5] suggests to construct a tree that balances the skew under the two given static thermal profiles (uniform and worst). The argument is that the skew optimized under one

thermal profile will vary significantly under the other profile, thus the need to balance. TACO first builds a nonbuffered, zero-skew clock tree under a uniform thermal profile and refines it under worst-case (non-uniform) profile.

TABLE I
INDEX TABLE FOR DEFINITIONS AND TERMS.

Variable	Definition
$\mathscr{C}$	Spatial correlation matrix.
$D_{(s_k)}$	Delay time from the source to sink k.
S_q	Steiner point q.
s_0	Source node.
$T(t,n)$	Temperature over the chip at time t for each node n.
$\hat{T}$	Mean-temperature for nodes n.
cc_p	Correlation coefficient in grid p.
M_j	Merging point j.
$d(M_j, s_k)$	Routing path from merging point j to sink k.
r_{unit}	Unit-length resistance.
s_k	Sink node k.
β	Temperature coefficient of resistance ($1/^oC$).
σ_i	Standard deviations for node i.

Since the thermal gradient is changing over time while the chip is running, a transient analysis/optimization is an extremely difficult task, if possible. Considering the skew caused by the spatial variation of temperature, PECO [5] is the only existing clock synthesis method considering time-variant variation by perturbation of embedding points.

With further merging points, PECO causes more wire length overhead. PECO has not discussed the skew variation issue, neither.

The skew variation problem can not be ignored in current very large scale integration (VLSI) technology. A smaller skew variation region, can lead to a more stable system and a more accurate timing analysis. This paper focuses on temperature variation induced skew and skew variation minimization. We propose a simultaneous hotspot avoid embedding and thermal aware routing (TMST) method to minimize skew variation and the worst case skew considering the on-chip temperature variation and spatial correlation with respect to operating time. The main contributions of this paper are as follow: First, without any extra components like crosslinks or buffers insertion, our proposed synthesis guarantee smaller wire-length which leads to small power consumption. Second, we build up clock tree embedding according to temporal and spatial temperature information makes our tree has smaller dynamic skew range (skew variations), our paper is the pioneer

one discussing this issue. Third, our method considers time-variant temperature variation using different kind of delay models. Among all the test, our TMST reachs not only the smallest skew but the smallest skew variation.

The rest of this paper is organized as below: Section 2 shows the notation and problem statement in this paper. Section 3 presents temperature modeling and delay model. Section 4 sums up the overall algorithms. We show our experimental results in Section 5 and conclude the paper in Section 6.

II. NOTATION AND PROBLEM STATEMENT

Table 1 shows the notations and definitions used in the following sections. Clock skew minimization is an important design task to ensure correct circuit behavior of sequential circuits, and many works have been done to design zero-skew clock tree. The main problem of design uncertainty is error of capacitance estimation. Even if we reduce design uncertainty by using detailed analysis and optimization, clock skew occurs due to manufacturing and environmental variabilities. This paper mainly focuses on temperature issue. There have been different proposed methods such as buffers and crosslink insertion for reducing skew. However, with further wire length or analogy elements, both crosslink and buffer insertion methods significant increase power consumption. Without any extra elements, our method reduces the skew by changing the essential routing path to further compensate skew and skew variation. We build up the entire tree topology and embedding in the high spatial and temporal correlated areas considering time variant temperature gradients. We also avoid routing through and building merging points on hot spot areas. High correlated area guarantees the same trend of temperature change, which leads to more smooth temperature grids.

Given a clock distribution topology generated by GDME, under the constraints below, we reembedding a new tree which has more high correlated routing paths and merging points.

- 1: We only implement our method with highly correlated sink pairs and keep the same path with GDME.
- 2: We build up our clock tree using a bottom-up fashion.
- 3: We avoid building our merging points and routing paths on Hot spot areas.
- 4: All routing paths and merging points are built on the highly correlated areas.

III. MODELING

A. Stochastic Temperature Model and Correlation Map

The same temperature modeling in [9] is assumed in this work. In order to make the paper self-contained, we first review the temperature, gradient and correlation model. The temperature gradient and correlation are obtained by a micro-architecture level power and temperature simulation [11], where the Alpha architecture is used as an example.

The overall chip is divided into a uniform grid with total N nodes. By applying six different applications (*ammp, art, compress, equake, gzip, gcc*) from the SPEC2000 benchmark in a sequence (each with a time-period t_p), the thermal-power

is obtained by averaging the cycle-accurate (scale of *ps*) dynamic power in the thermal-constant scale (scale of *ms*). Using this time-variant thermal power as input, the transient-temperature $T(t_i, n_j)$ over the chip is calculated at different time-instant t_i for each node n_j in the grid. To automatically extract correlation for temperature variations, the temperatures at N nodes are modeled by random processes. Each node is described by a temperature sequence sampled at $\mathcal{N}$ time-instants,

$$\mathscr{S}_{n_1} = \{T(t_1, n_1), ..., T(t_p, n_1), T(t_{p+1}, n_1), ..., T(t_{\mathcal{N}}, n_1)\}$$
$$\mathscr{S}_{n_2} = \{T(t_1, n_2), ..., T(t_p, n_2), T(t_{p+1}, n_2), ..., T(t_{\mathcal{N}}, n_2), ...\}$$
$$...$$
$$\mathscr{S}_{n_N} = \{T(t_1, n_N), ..., T(t_p, n_N), T(t_{p+1}, n_N), ..., T(t_{\mathcal{N}}, n_N)\}$$

a temperature (spatial) correlation matrix is defined by

$$\mathscr{C}(i, j) = \frac{cov(i, j)}{\sigma_i \cdot \sigma_j}, \tag{1}$$

where

$$cov(i, j) = \sum_{k=1}^{\mathcal{N}} T(t_k, n_i) T(t_k, n_j) - \sum_{k=1}^{\mathcal{N}} T(t_k, n_i) \sum_{k=1}^{\mathcal{N}} T(t_k, n_j) \tag{2}$$

is the co-variance matrix between nodes,

$$\sigma_i = \sqrt{\sum_{k=1}^{\mathcal{N}} T(t_k, n_i)^2 / \mathcal{N} - (\hat{T}_i)^2}, \quad \sigma_j = \sqrt{\sum_{k=1}^{\mathcal{N}} T(t_k, n_j)^2 / \mathcal{N} - (\hat{T}_j)^2} \tag{3}$$

are the standard deviations for nodes n_i and n_j, and

$$\hat{T}_i = \sum_{k=1}^{\mathcal{N}} T(t_k, n_i) / \mathcal{N}, \quad \hat{T}_j = \sum_{k=1}^{\mathcal{N}} T(t_k, n_j) / \mathcal{N}. \tag{4}$$

are mean-temperature for nodes n_i and n_j respectively. The correlation coefficients $\mathscr{C}(i, j)$ can be precomputed and stored into a table. Figure 1 shows the distribution of one calculated correlation matrix. The averaged correlation is about 0.8 for the SPEC2000 benchmarks [9].
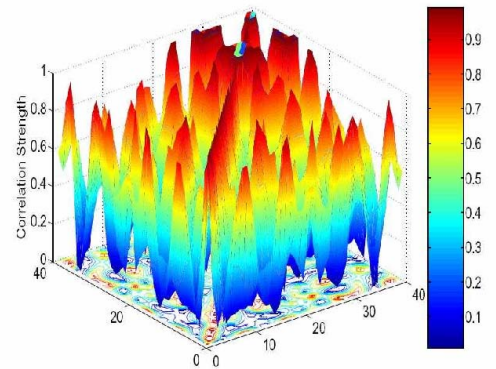

Fig. 1. Temperature correlation matrix from running sequent of SPEC2000 benchmarks.

B. Skew Model with Temperature Variation

As suggested by [5], when a clock wire experiences a temperature gradient, the unit-length resistance r_{unit} is as follows,

$$r_{unit}(x,y,t) = \rho_0 \cdot [1 + \beta \cdot T(t,x,y)], \qquad (5)$$

where ρ_0 is the unit-length resistance at 0^oC, and β is the temperature coefficient of resistance $(1/^oC)$. When the embedding path $d(M'^i, s_k)$ is fixed, we calculate the new resistance by

$$R(M'^i, s_k) = \sum_{\forall e \in d(M'^i, s_k)} E[r_{unit}(e)] \cdot len(e) \qquad (6)$$

where $E[r_{unit}(x,y)]$ is the mean value of resistance in edge e (M'^i, s_k)

Following the conventional definition for the propagation delay, the delay from the source node s_0 to sink s_i, $D_{(s_0 \rightsquigarrow s_i)}$, is the time required for the node voltage (waveform) to pass 100% of the peak voltage under the impulse excitation in the source node. After obtaining the source to sink delay of j-th routing configuration $Conf_j^i$ in level i, we can calculate the worst case skew corresponding to $Conf_j^i$ as follows

$$Skew_i = \max_{\forall \text{ sink } s_k} D_{(s_0 \rightsquigarrow s_k)} - \min_{\forall \text{ sink } s_k} D_{(s_0 \rightsquigarrow s_k)}. \qquad (7)$$

The worst-case skew is then determined by those preserved routing path from all levels.

C. Problem Formulation

The simultaneous hotspot avoid embedding and thermal aware routing (TMST) problem is formulated as follows,

Formulation 1: (Simultaneously hotspot avoid embedding and thermal aware routing (TMST)) Given source s_0, sinks $s_1 \cdots s_n$, an initial clock tree embedding, and a set of temperature variation maps, find proper re-embedding (including merging point and re-routing) for the new tree to minimize the worst case skew under the given temperature maps.

IV. ALGORITHMS

A. Overall Algorithm

Given a GDME-initialized clock tree construction, the re-embedding by thermal aware Maze routing is performed. The worst-case skew and re-embedding are determined in a bottom-up fashion. At each level, the merging points and routing paths are picked according to their correlation strength. Then the resulting routing path are routed through with strong correlation area, and only those sink paths that could cause large skew changes (high correlated) are selected for re-embedding.

In summary, the overall algorithm is shown in Figure 2, and the algorithm's pseudo code is as presented in algorithm 1:
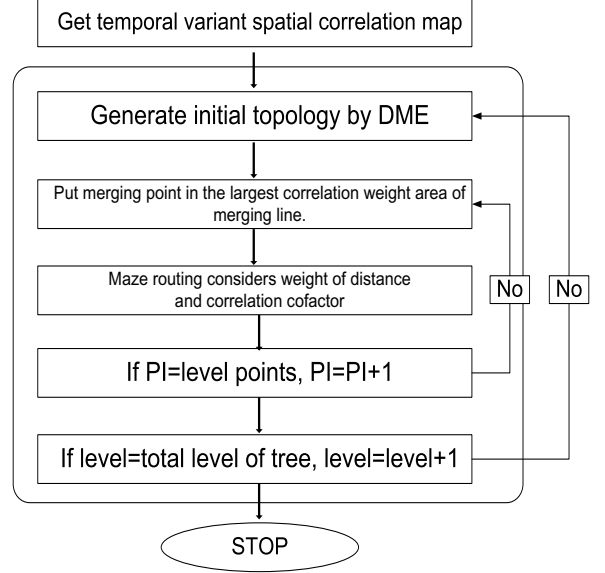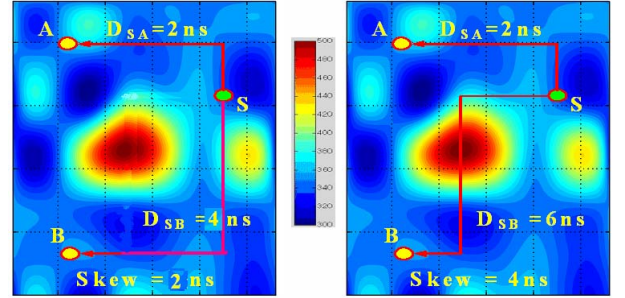

Fig. 2.   Top view of overall algorithm

Fig. 3.   Different routings cause different delays.

B. Correlation Cofactor

Smoother routing path guarantees more stable skew variation since the dynamic temperature variation over time generate different skews. The Thermal Aware Routing Topology Optimization (TMST) is an effective algorithm that considers the time variant temperature variations with spatial and temporal correlation. TMST generates a temperature correlation map by analyzing time variant temperature maps, and avoid the hot spots that are indicated in the temperature correlation map of the clock tree structure. Without using merging point perturbation, we use thermal aware routing to balance the skew, which can still keep the same or similar Manhattan distance. First, we build a macro model for temperature variations to get temperature maps for various timestamps. To model such on-chip time variant temperature, we impose a grid onto the chip and each grid is assigned a temperature range. This temperature range can be obtained by measurement or thermal simulation. A complete instruction set is tested and the corresponding K temperature profiles are obtained. The overall temperature variation can then be obtained based on
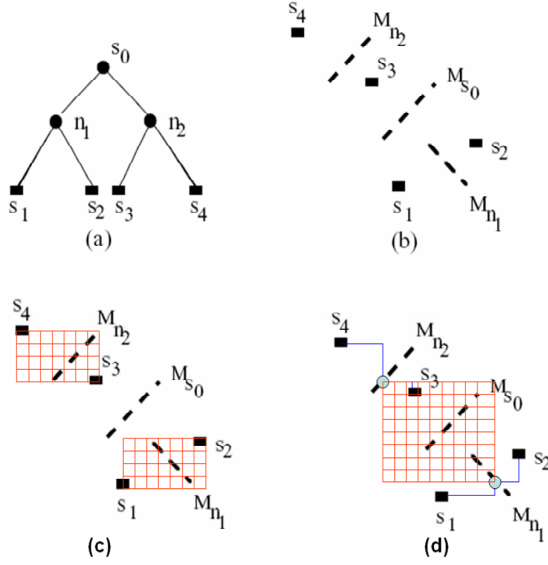
Fig. 4. Overall flow

Algorithm 1 TMST

Input: Source s_0, sinks $s1, \cdots, sn$.

Output: A modified embedded clock tree T' {Bottom up embedding from the second last level to the second level}

1: Acquire temporal variant spatial correlation map
2: **while** $L_i != Level$ **do**
3:     Generate initial embedding tree by GDME
4:     **while** $p_i^j != PC_i$ **do**
5:         Find the merging segment
6:         Choose the largest correlation weight area but not hotspot as the merging point
7:         Apply thermal aware Maze routing to find the highest correlated path.
8:         $j = j + 1$
9:     **end while**
10:    $i = i + 1$
11: **end while**
12: **return** T'

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the K temperature profile.

Because of the linear relationship between wire resistance and temperature, high temperature variance can increase the delay by as much as 100%. Therefore, it is necessary to find a routing path with smooth temperature gradient in order to avoid clock skew that is created by temperature variations.

To find a suitable enable cofactor in thermal aware routing, we use "correlation cofactor" in each of the two target points we want to analyze. Different from correlation coefficients, correlation cofactor in area p to targets i, j is defined as the sum of corresponding two correlation coefficients $cc_p = cov(i, p) + cov(p, j)$. The area with high correlation cofactor value represents high correlation with both routing target points. TMST method tries to build up the entire tree in the

areas with high correlation cofactor values which leads the clock tree with better thermal tolerance. Further avoidance of hot spot areas can further reduce the worst case skew.

Definition 1: Correlation cofactor in area p to routing point S, T is defined as the sum of corresponding two correlation coefficients $cc_p = cov(S, p) + cov(p, T)$.

C. Thermal Aware Maze With Dynamic Window

High temperature variability greatly impacts the delay and skew of the zero-skew clock tree. Figure 3 shows that different routing paths with different temperature gradients will have different skews. The high temperature variance increases the delay by 100%, i.e., from 2*ns* to 4*ns*. In Figure 3, on the one hand, we can see the subregion with high temperature. On the other hand, we also notice that we can find the path with smooth temperature gradient but keep the short wire length as well.

Routing is a crucial step in clock tree synthesis design. Most of existing thermal aware clock tree synthesis uses roughly Manhattan distance to simulate and evaluate the delay between each two nodes [6], [9]. In real case, Manhattan distance is not exactable when considering time-variant temperature maps if our objective function consider both weight of temperature and distance parameters. We use *thermal aware routing Maze Routing* with considering both distance and temperature correlation cofactor in this paper, which not only is an accurate method for evaluating the delay between each node but also can reduce the skews and skew variation significantly. However, not all path with high correlation lead better thermal toleration ability. With two fully components temperature difference path sometimes cause better skew reduction. In order to choose suitable path candidates, we only target path according to sink point correlation strength in this paper.

D. Overview

As shown in Figure 4(a), we get the initial tree from GDME topology. Unlike GDME, we build the small dynamic window with each candidate pair before designing merging point and routing path. Dynamic windows are small grids with weight of spatiotemporal information. We determine the routing paths and merging paths based on dynamic windows level by level as shown in Figures 4(c) and (d).

Figure 5 presents a short overview on how to build up the dynamic windows. The green spots are the sinks of the clock tree, and the stars are the hotspot areas.

For grid j, its correlation coefficient related to sink k is 0.25. Its correlation coefficient related to sink i is also 0.25. The sum of these two coefficients is the correlation cofactor between these two sinks, which is 0.5 in this case. Only the correlation coefficients of the grids that are inside of the dynamic window of two sinks are calculated. After obtaining the correlation coefficients, we find the merging segment by calculating the Manhattan distance. We determine the merging point by avoiding the hot spots and search for the grid with the highest correlation coefficient on the merging segment. In this grid map, the highest correlation coefficient
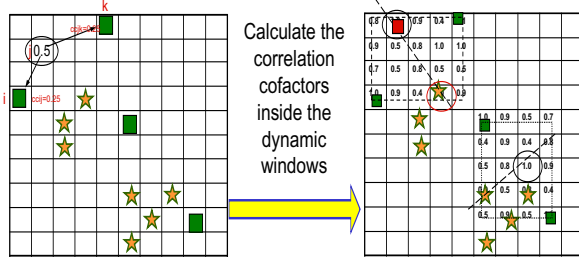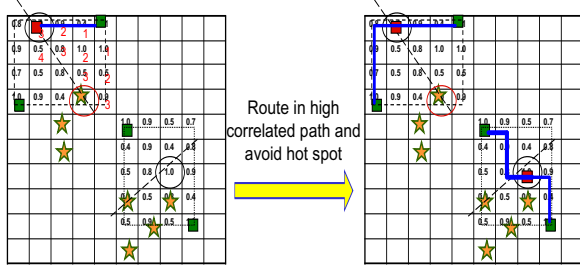
Fig. 5. Dynamic windows

Fig. 6. Determine the routing path

is 1, but it is in the hotspot area. Instead of choosing the highest correlation coefficient area, we choose the next highest correlation coefficient as our merging point in order to avoid the hotspot. As illustrated in figure 6, after choosing the merging point, we apply thermal aware Maze Routing to select the highest correlated path, while mantaining the same Manhattan distance.

V. EXPERIMENTAL RESULTS

The proposed algorithm has been implemented in C++ programming language and Matlab. We report runtime using a Linux workstation with 1.9GHz, P4-CPU, and 2GB memory. We employ the standard clock-tree benchmarks r1-r5 which are the same benchmarks in TACO and PECO. Two more industry cases JPEG1 and JPEG3 are tested in this paper. The initial zero-skew tree is constructed by the GDME [4] method under the Elmore delay model with no temperature variation. The interconnect has unit resistance $r_0 = 0.1\Omega/mum$, unit capacitance $c0 = 2.0 \times 10^{-16}F/\mu m$, and temperature sensitivity $\beta = 0.0068$, The above interconnect parameters are the same as those in TACO [6].

A chip with size of $6cm^2$ is divided into a uniform grid to obtain the distributed temperature map by a micro-architecture level cycle-accurate power /temperature simulator [11]. Our experiments use six *SPEC*2000 applications (*art, ammp, compress, equake, gcc, and gzip*). We collect 100 temperature maps by simulating these applications in a sequence and recording temperature maps for every 10 million clock cycles after fast forwarding of 1 billion cycles. These applications lead to a temperature variation about 50^oC over the 100

TABLE II
PATHLENGTH SKEW COMPARISON

Input (node)	[4](ps)	TACO(ps)	PECO(ps)	TMST(ps)
r1(267)	0	10.8	7.97	4.175
r2(598)	0	374.9	367.8	194.5
r3(862)	0	588.3	561.7	242.9
r4(1903)	0	621.1	571.6	209.6
r5(3101)	0	1124.4	1311.4	564.8
JPEG1(3603)	0	1384.1	1437.5	720.48
JPEG2(10.3K)	0	2097.3	2286.4	1577.3

TABLE III
SKEW VARIATION COMPARISON

Input (node)	[4] (ps)	TACO(ps)	PECO (ps)	TMST (ps)
r1(267)	22.2	24.5	21.3	9.5
r2(598)	32.9	33.8	34.8	13.4
r3(862)	33.2	34.8	34.5	14.5
r4(1903)	41.3	43.2	44.2	27.3
r5(3101)	78.6	77.9	54.1	35.3
JPEG1(3603)	82.6	84.5	77.3	37.4
JPEG2(10.3K)	197.6	208.8	209.4	88.5

temperature maps. We then find regions of hot spot with high temperature variation (variance), and extract correlation matrix, i.e., covariance for pairwise regions. Below, we report the minimum-cost bounded-skew routing tree problem under the pathlength (linear) delay models in table II. Compared with existing temperature-aware clock tree method, our TMST solution reduces skew variation by 2X compared with the Greedy-DME (GDME) method of Edahiro and existing thermal aware clock synthesis TACO and PECO. With the scale from 100 down to 1 temperature maps, our TMST also guarantees the smallest wirelength overflow. TMST reduces worst case skew up to 4X than PECO and 5X than TACO.

A. Comparison With Existing Techniques

We show the skew comparison with linear delay model in table II. GDME gets zero skew since it build up tree in H shape. TMST gets the best pathlength skew delay in all comparison. Table 4 shows the run-time comparison between different algorithms. We do detail routing with each two connecting pairs instead of roughly Manhantan distance, and further accurate high order delay model, TMST consumes much run time cost compared with other existing methods.

Table V compares our proposed TMST with the existing techniques GDME [3], and thermal aware clock synthesis PECO [9] and TACO [6] with SPICE. We scale from 100

TABLE IV
RUN TIME COMPARISON

Input (node)	[4] (s)	TACO (s)	PECO (s)	TMST (s)
r1(267)	0.5	3	4.5	79
r2(598)	1.0	10	7.9	231
r3(862)	1.4	18	19.1	498
r4(1903)	2.1	55	73.8	621
r5(3101)	4.5	121	233.4	766
JPEG1(3603)	5.1	144	299.7	988
JPEG2(10.3K)	8.1	238	501.2	1638

TABLE V

COMPARISON BETWEEN TMST AND EXISTING SKEW REDUCTION TECHNIQUES

Input(node)	wirelength(m)				w-skew-SPICE (100-map)(ps)				wirelength over(%)			TMST skew imprv(X)		
	[4]	TACO	PECO	TMST	[4]	TACO	PECO	TMST	TACO	PECO	TMST	[4]	TACO	PECO
r1(267)	1.32	1.32	1.34	1.33	145.1	132.7	109.7	23	0.01	1.5	0.7	6.3	5.76	4.76
r2(598)	2.59	2.64	2.62	2.62	534.5	289.4	162.6	53	1.9	1.1	1.1	10.1	5.46	3.06
r3(862)	3.38	3.41	3.43	3.41	582.3	391.3	203.1	64.8	0.88	1.4	0.88	8.99	6.04	3.13
r4(1903)	6.81	6.84	6.84	6.83	1424	831.3	165.8	126.5	0.44	0.44	0.29	11.26	6.57	1.31
r5(3101)	10.2	10.3	10.3	10.3	3533	1973	1324	339.4	0.98	0.98	0.98	10.4	5.8	3.9
JPEG1(3603)	9.31	9.33	9.35	9.33	1447	1211	1458	423.3	0.21	0.43	0.21	3.42	2.9	3.4
JPEG2(10.3K)	43.1	44.3	44.3	44.3	4755	3211	2455	2421	2.7	2.8	2.7	1.9	1.3	1
Input(node)	wirelength(m)				w-skew-SPICE (50-map)(ps)				wirelength over(%)			TMST skew imprv(X)		
	[4]	TACO	PECO	TMST	[4]	TACO	PECO	TMST	TACO	PECO	TMST	[4]	TACO	PECO
r1(267)	1.32	1.33	1.37	1.32	144.2	130.8	108.3	22	0.75	3.78	0.01	6.5	5.9	4.9
r2(598)	2.59	2.62	2.63	2.61	527.8	288.4	161.9	50	1.1	1.5	0.77	10.5	5.7	3.2
r3(862)	3.38	3.46	3.44	3.46	581.4	389.7	179.8	60.8	2.3	1.8	2.3	9.6	6.4	2.9
r4(1903)	6.81	6.84	6.85	6.82	1423	827.6	164.5	125.9	0.44	0.58	0.14	11.3	6.5	1.3
r5(3101)	10.2	10.4	10.5	10.3	3521	1955	1302	331	1.9	2.9	0.98	10.6	5.9	3.9
JPEG1(3603)	9.31	9.34	9.34	9.33	1438	1209	1439	419	0.32	0.32	0.21	3.4	2.9	3.4
JPEG2(10.3K)	43.1	43.3	44.2	43.5	4750	3208	2443	2413	0.46	2.5	0.93	1.97	1.3	1
Input(node)	wirelength(m)				w-skew-SPICE (20-map)(ps)				wirelength over(%)			TMST skew imprv(X)		
	[4]	TACO	PECO	TMST	[4]	TACO	PECO	TMST	TACO	PECO	TMST	[4]	TACO	PECO
r1(267)	1.32	1.35	1.37	1.32	143.2	129.4	107.3	22	2.27	3.7	0.02	6.5	5.8	4.8
r2(598)	2.59	2.62	2.61	2.61	519.1	278.7	161.8	48	1.15	0.77	0.77	10.8	5.8	3.3
r3(862)	3.38	3.45	3.44	3.39	579.5	379	178.9	51.7	2.3	1.7	2.3	11.2	7.3	3.4
r4(1903)	6.81	6.84	6.85	6.82	1420	819.6	163.2	124.8	0.44	0.59	0.14	11.4	6.57	1.3
r5(3101)	10.2	10.4	10.5	10.3	3500	1949	1297	327	1.9	2.9	0.98	10.7	5.96	3.97
JPEG1(3603)	9.31	9.34	9.34	9.33	1427	1209	1437	418	0.32	0.32	0.21	3.41	2.8	3.4
JPEG2(10.3K)	43.1	43.3	44.3	43.8	4755	3201	2447	2418	0.46	2.5	0.92	1.97	1.32	1
Input(node)	wirelength(m)				w-skew-SPICE (2-map)(ps)				wirelength over(%)			TMST skew imprv(X)		
	[4]	TACO	PECO	TMST	[4]	TACO	PECO	TMST	TACO	PECO	TMST	[4]	TACO	PECO
r1(267)	1.32	1.35	1.37	1.33	142.3	123.3	102.2	21	2.3	3.8	0.75	6.78	5.87	4.87
r2(598)	2.59	2.61	2.63	2.62	511.1	279.5	161.3	44	0.77	1.54	1.15	11.7	6.35	3.67
r3(862)	3.38	3.39	3.43	3.38	579.5	386	177.3	52.3	0.29	1.47	0.01	11.1	7.4	3.4
r4(1903)	6.81	6.84	6.88	6.83	1431	827	163.3	125.3	0.44	1	0.29	11.4	6.6	1.3
r5(3101)	10.2	10.4	10.8	10.3	3523	1948	1289	330	1.96	5.9	0.98	10.7	5.9	3.91
JPEG1(3603)	9.31	9.33	9.34	9.32	1427	1199	1422	409	0.21	0.32	0.1	3.49	2.9	3.48
JPEG2(10.3K)	43.1	44.3	44.2	43.4	4732	3208	2189	2218	2.78	2.5	0.69	2.13	1.45	0.98
Input(node)	wirelength(m)				w-skew-SPICE (1-map)(ps)				wirelength over(%)			TMST skew imprv(X)		
	[4]	TACO	PECO	TMST	[4]	TACO	PECO	TMST	TACO	PECO	TMST	[4]	TACO	PECO
r1(267)	1.32	1.34	1.34	1.34	144.1	121.8	108.3	21	1.5	1.5	1.5	6.87	5.8	5.16
r2(598)	2.59	2.61	2.62	2.63	521.1	275	130.4	39	0.77	1.15	1.5	13.36	7.1	3.3
r3(862)	3.38	3.39	3.41	3.45	586.3	379	169.3	48.5	0.29	0.89	2	12.1	7.8	3.49
r4(1903)	6.81	6.84	6.86	6.85	1397	817.4	173.3	98.3	0.44	0.73	0.59	14.2	8.31	1.76
r5(3101)	10.2	10.4	10.4	10.3	3500	1944	1297	298	1.96	1.9	0.98	11.7	6.5	4.36
JPEG1(3603)	9.31	9.33	9.35	9.32	1427	1207	1437	408	0.21	0.43	0.01	3.5	2.96	3.5
JPEG2(10.3K)	43.1	44.3	44.1	43.4	4741	3204	2439	1911	2.8	2.3	0.69	8.48	1.68	1.28

maps down to 1 temperature map. Our TMST has the best skew reduction in all of testing cases.

Table V also reports wirelength for different algorithms, where runtime includes the time to build macromodel for PECO and TMST.

We present the skew violation distribution of r4 in Figure 7 and Figure 8, note that our TMST has not only small worst case skew but also small skew variation.

Figure 9 shows the clock tree built by our TMST method in JPEG1 case. Significant bending in the route between nodes can be seen.

VI. CONCLUSIONS AND FUTURE WORK

Existing clock tree and hybrid clock synthesis did not consider extra skew caused by temperature variation, or [8] needed to assume a time-invariant worst-case temperature map to find the worst-case skew. Those papers also use Elmore delay model to evaluate clock skew. In this paper we have made the first attempt to reduce skew variation considering time variant temperature variation. We have developed a minimal skew clock tree embedding that considers temporal and spatial correlation issue. Thermal aware routing topology optimization is used to avoid hot-spots and compensate temperature variation. With the entire tree in the smoother temperature areas, our tree synthesis can significant reduce the skew variation and worst case skew. Compared with existing temperature-aware clock tree methods, our TMST solution reduces skew variation by 2X compared with the Greedy-DME (GDME) method of Edahiro and existing thermal aware clock synthesis TACO and PECO. With the scale from 100 down to 1 temperature maps, our TMST also guarantees the smallest wirelength overflow. TMST reduces worst case skew up to 4X than PECO and 5X than TACO.
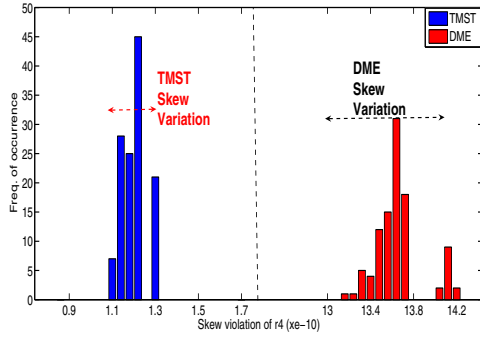
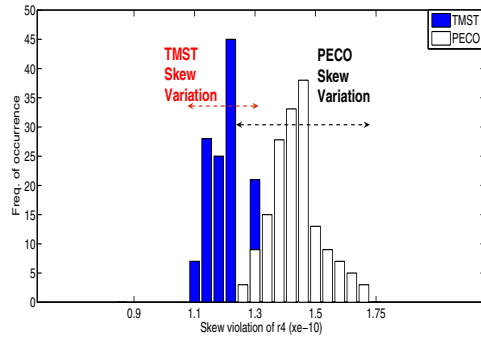Fig. 7.   Skew violation range (skew variation) of r4 (GDME and TMST)

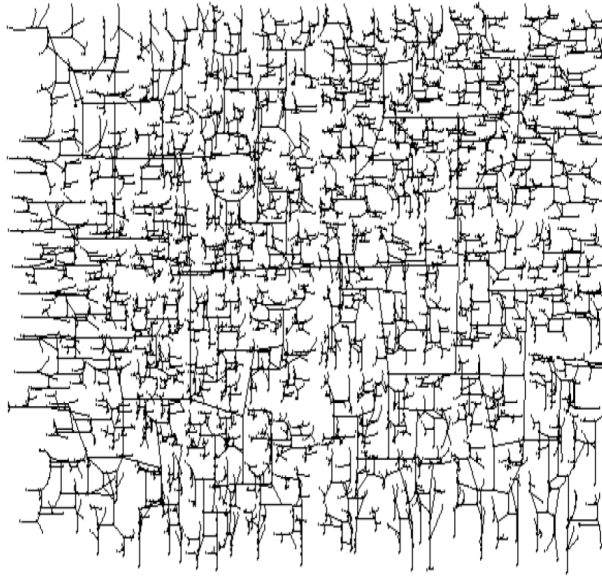Fig. 8.   Skew violation range (skew variation) of r4 (PECO and TMST)

Fig. 9.   Clock routing tree after TMST for JPEG1

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