Comparative Analysis of NBTI Effects on Low Power and High Performance Flip-Flops

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***Abstract*— Mitigating the circuit aging effect in digital circuits has become a very important concern for current and future technology nodes. Negative Bias Temperature Instability (NBTI) is one of the most important circuit aging mechanisms, which can incur timing errors. Flip-flops play a vital role as storage elements in pipelined architectures and are prone to effects of aging. NBTI increases the transistor threshold voltage, affecting the performance of the chip. In this paper, we study the effects of NBTI on the timing characteristics of different types of low power and high performance flip-flops. Factors such as input data probability and temperature which affect the degradation rate are also analyzed.**

I. Introduction

As technology continues to scale, circuit reliability has become dominant design factor. Reliability concerns manifest themselves as either timing errors caused by mechanisms like Negative Bias Temperature Instability (NBTI) and Hot Carrier Injection (HCI) or hard failures due to Electromigration and Time-dependent dielectric breakdown (TDDB) rendering the chip unusable.

Negative Bias Temperature Instability (NBTI) is projected to have a huge impact on the performance of digital circuits over a period of time. Timing violations occur due to the increased threshold voltages (V_{th}) and decreased on-current (I_{on}) of the PMOS transistors in the circuit. The reduced speeds of the logic gates due to NBTI result in reduced performance eventually leading to timing violations as the circuit ages [1][2][3]. NBTI occurs due to the trap generation at the Si-SiO_2 interface in the PMOS transistor when it is in inversion (V_{gs} = -V_{dd}). As the result of interface trap generation, the on-current (I_{on}) decreases and threshold voltage (V_{th}) increases resulting in decreased performance of the device. Fortunately, when the transistor is in cut-off region, annealing of these traps occur which results in recovery of the lost threshold voltage.

Flip-flops are one of the most important structures in a micro-processor. Flip-flops are clocked storage elements which hold the states in sequential circuits sampled at a preferred clock edge [4]. They play a vital role in the design of synchronous circuits and clocking of the system. The timing characteristics of the flip-flops decide the frequency of operation of the circuit. Thus, it is imperative for the flip-flop timing characteristics to be unperturbed by external factors such as variations and aging. In this paper, we study the effect of NBTI on the timing characteristics of various low power and high performance flip-flops.

NBTI has different effects on combinational and memory circuits and they have been widely studied by various researchers in [5][6]. Various methods such as transistor up-sizing and gate replacement techniques for combinational circuits have been proposed in [5]. Performance evaluation and reduction in static noise margin (SNM) of memory circuits due to NBTI have been done in [6]. Adaptive body biasing has been shown as a promising compensation technique to combat NBTI in [7]. Onchip monitors to compute the degradation due to NBTI have been proposed in [7] and [8]. [9] claim that sequential circuits are not affected by NBTI. However, authors in [10] have shown it to be a problem and that up-sizing the NBTI prone transistors increase the lifetime of the flip-flops. However, they consider the input data probability as 0.5 which does not exhibit the worst case condition as shown in the later sections. The major contribution of this work is a comprehensive analysis of the timing characteristics of the various low power and high performance flips-flops affected by NBTI. This analysis will help the designers in choosing the right flip-flop judiciously during the design time ensuring long term reliable circuits.

The rest of the paper is organized as follows. Section II talks about the background of NBTI, flip-flop timing metrics and the motivation behind this work. Section III talks about the various topologies of flip-flops. Our experimental setup and results are discussed in section IV and we conclude in section V.

II. Background & Motivation

A. Negative Bias Temperature Instability (NBTI)

NBTI is growing to be a major reliability threat in the nanometer regime. NBTI causes an increase in the absolute threshold voltage of the PMOS transistors. The most commonly explained theoretical framework for NBTI is the Reaction-Diffusion (R-D) model explained in [1]. R-D model has two critical steps for NBTI. Reaction is the process at which the Si-H and Si-O bonds at the substrate/gate oxide interface are broken during the negative bias ($V_{gs} = -V_{dd}$) and the interface traps are generated. The generation rate is an exponential function of electrical field, temperature and the density of reaction species. The threshold voltage

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increases during the process of reaction. Diffusion is the process in which the device is OFF ($V_{gs} = 0$) and the generated species diffuse towards the gate thus reducing the change the threshold voltage [2]. We use the long term threshold degradation model explained in [2][3] to calculate the change in threshold voltage of a PMOS transistor.

$$\Delta V_{th} = (\sqrt{K_v^2.T_{clk}.\alpha/(1-\beta_t^{1/2n})})^{2n} \quad (1)$$

where

$$\beta_t = 1 - \frac{2.\xi_1.t_e + \sqrt{\xi_2.C.(1-\alpha).T_{clk}}}{2.t_{ox} + \sqrt{C.t}} \quad (2)$$

Equation 1 calculates the ΔV_{th} of a degraded PMOS device where K_v is a function of electrical field, temperature and carrier concentration, n is the time exponential constant equal to 0.16, α (SP) is the signal probability of the input. α is the total amount of time the input to the PMOS transistor is LOW (Logic '0'). Note that the input data probability (DP) is the probability of the input D being HIGH (Logic '1') is equal to 1-α and henceforth, we will use DP for our illustration purposes.Figure 1 shows the change in threshold of a 65nm PMOS device over 5 years for various values of DP.

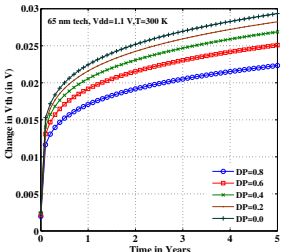

Fig. 1. V_{th} degradation for 65nm technology for various input data probabilities (DP)

B. Flip-Flop Timing Metrics

The important timing metrics of flip-flops for consistent estimation of various parameters are inter-dependent and well-established metrics which are explained in [11] [12]. Figure 2 shows the important timing parameters of sequential elements. T_{cq} of the design increases monotonously as the data arrives close to the clock edge before the absolute setup time after which the operation fails. The region of failure as shown in figure 2 is the region when the input D changes from one state to another which results in latching of wrong output. T_{sua} and T_{ha} are the absolute values of setup and hold time beyond which faulty operation occurs. It is not unusual for a flip-flop to have negative setup time and zero hold time due to it's topology and design. Violation of a setup time constraint results in latching the wrong value on to the sequential element and can be rectified by decreasing the clock frequency. Hold time violations cannot be rectified and renders the chip useless. Buffers are usually added to increase the delay to eliminate hold time violations.

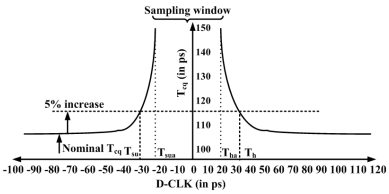

Fig. 2. Typical timing characteristics of a flip-flop

C. Motivation

The minimum time period for the clock governing a pipeline stage with flip-flops has to satisfy equation 3 for correct operation.

$$T \geq T_{ff} + T_{logic} + T_{skew} \quad (3)$$

where T is the clock period, T_{logic} is the combinational logic delay between two pipeline stages and T_{skew} is the clock skew and T_{ff} = T_{su} + T_{cq}, where T_{su} is the setup time and T_{cq} is the CLK-Q delay. Various approaches are followed to set the value of T_{su} which is used to compute the value of T_{ff}. One approach is setting the setup time as the point at which T_{cq} is 5 or 10% more than the nominal T_{cq} as shown in figure 2. Another approach maintains the optimal setup time as the point at which T_{dq} is minimal as shown in figure 3 [12][13]. In this work, we analyze both the cases. We define case 1 as the approach where the setup and hold times of the design are set at the point of 5% increase in T_{cq} of the nominal value. The point of minimal T_{dq} is represented as case 2. The value of T_{ff} is dependent on the type of transition of the output (0→1 or 1→0) and is taken as the maximum of both the transitions. In this paper, we have shown both the cases for explanatory purposes. The worst case conditions occur when there is no combinational logic between the two elements and the internal race immunity is shown in equation 4.

$$T_{cq} \geq T_h + T_{skew} \quad (4)$$

From equations 3 & 4, it is clear that the clock period is determined by T_{ff}. Equation 3 includes the worst case timing of T_{ff} for combinational logic delay for all operating conditions. Therefore, it is important to reduce T_{ff} which the flip-flop uses from the clock cycle to achieve higher performance. It should also be noted that as the data arrives closer to the clock edge, T_{cq} increases. Thus, the data cannot be allowed to arrive closer to the clock edge than the pre-determined time as this may result in increased T_{su} & T_{cq} which will result a wrong operation due to violation of equation 3. Due to NBTI, the data arrives later than expected due to the increase in the combinational logic delay which is also severely affected due to NBTI. So, it is imperative to understand the response of flip-flops to both late arriving signals and self degradation.

In figure 3, we observe that the T_{cq} of an aged Transmission Gate Master-Slave Flip-Flop (TG-MSFF) increases as time progresses. The absolute increase in the T_{cq} increases T_{ff} and thereby increases T in equation 3. Thus, we observe that under the worst case conditions, the minimum time period T in equation 3 could be violated making the pipeline stage faulty. The degradation due to NBTI is dependent on the input signal probability as seen from figure 1 and is explained in section IV. Thus, it is imperative to analyze the impact of NBTI on various high performance and low power flip-flops under various conditions.

III. Topologies

A. Topologies

Flip-flops come in various forms depending on whether they are used in high performance or low power designs. In

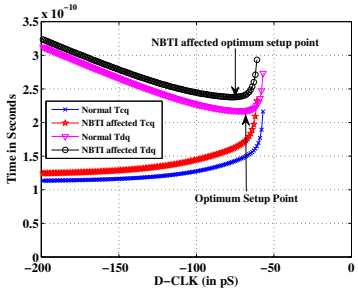

Fig. 3. Timing characteristics of a TG-MSFF

this section, we describe the designs of four such flip-flops used in commercial processors.

1) Master-Slave Latch Pairs: A flip-flop can be designed using a pair of latches when one is Transparent High (TH) and the another one is Transparent low (TL). Figure 4 (a) shows the setup of a Transmission Gate Master-Slave Flip-Flop (TG-MSFF). Figure 4 (b) shows the design of a modified clocked CMOS master-slave flip-flop (C^2MOSFF). This is a modified version of a standard dynamic C^2MOSFF for lower power consumption. Both of these are low power flip-flops. They have high T_{cq} and T_{dq} compared to pulse triggered latches explained later. Both of these latches are used in low power designs where speed penalty can be incurred.

2) Pulse Triggered Latches: Pulse triggered latches can be considered as master-slave latches with very small transparent window. The master latch serves as the pulse generator while the slave latch captures the input. Here, we have analyzed two such pulse triggered latches namely Hybrid Latch Flip-Flop (HLFF) and Semi-Dynamic Flip-Flop (SDFF). HLFF proposed by Partovi in [14] was used in AMD K6 and has extremely small delay with static pulse generation mechanism. Meanwhile, SDFF has a static and dynamic pulse method with a dynamic pulse generator feeding the static latch [15]. Pulse triggered latches are extremely fast flip-flops with very small delay. However, they consume high power due to internal switching power due to it's precharge and evaluate operation.

IV. Experimental Results & Discussions

All the designs shown in figure 4 were simulated using Predictive Technology Models (PTM) [16] using HSPICE. We use the in-built Levenberg-Marquardt algorithm in HSPICE for optimal gate sizing for the minimum power-delay product (PDP). The algorithm uses steepest descent and Gauss-Newton method for optimization. Nominal rise and fall slopes for the clock was provided along with a standard load capacitance of FO4 inverters. All the transistors are sized at minimum length (L=1) while the widths are optimized. The simulations were run for a frequency of f_{clk}=1 GHz. The duty cycle of the clock was 50% with nominal temperature at 80° Celsius and the input is allowed to switch maximum of only once during a single clock cycle. We assume that the clock signals CLK and $\overline{CLK}$ do not suffer from clock skew. The base designs were simulated in 65nm technology and we use a supply voltage of V_{dd}=1.1V.

In this section, we present the set of results for each flip-flop. The threshold degradation of each PMOS transistor in the design is obtained using equations 1 and 2 depending on the amount of time they were stressed. The metrics are obtained with the setup and hold skews to be optimistic (long enough)The results are presented for a dynamic circuit operation of 5 years.

The effect of NBTI is dependent on the amount of time the device is stressed. This stress time is dependent on the data input probability DP (DP=$1-\alpha$) and is shown in the figure 1. In the following section, we also illustrate how the flip-flop timing characteristics vary with this parameter. The effect of transistor stacking on NBTI as explained in [17] should also be taken into account for proper characterization of the effects.

A. Master-Slave Latch Pairs

NBTI in a PMOS transistor increases the rise time of a $0 \rightarrow 1$ transition and lowers (negligible) the $1 \rightarrow 0$ transition when used in a pull-up network (PUN). TG-MSFF exhibit positive setup and negative hold times. Since, the hold time is negative for both the nominal and NBTI affected designs, we present only the other timing metrics here for the design. Figure 5 shows the input data probability has a considerable impact on CLK-Q T_{cq} and setup time T_{su}The setup time of the TG-MSFF in figure 4 (a) is dependent on TG1 and the set of inverters I1, I2 of the master latch. The CLK-Q delay T_{cq} is dependent on TG3 and the set of inverters I3 and I4 of the slave latch. The absolute setup time T_{sua} in figure 5 also increases as DP increases. The increase in T_{cq} for $1 \rightarrow 0$ transitions (shown in the inner figure) shows marginal change and is insignificant compared to $0 \rightarrow 1$ transition and does not contribute to maximum T_{ff}.

Due to the dynamic nature of the transmission gates along with the clock input of 50%, they undergo less stress than a constantly stressed static gate. Accounting for the correct stress in transmission gates, the degradation of T_{ff} due to NBTI for various input data probabilities is calculated. Figure 6 shows the increase in T_{ff} of a NBTI affected flip-flop if the signal arrives at the setup time (case 1) decided for the unaged flip-flop for both the transitions. Such an increase in T_{ff} can result in violation of the condition for T in equation 3. The design is affected the most for the input data probability of DP=1 (input remains '1' all the time). We observe a decrease in T_{cq} for DP=0 (which means input is '0' all the time) since this does not affect the PMOS in I4 and the completely stressed PMOS in I3 helps in the transition of $1 \rightarrow 0$.

Figure 7 shows the value of T_{ff} in equation 3 after degradation due to NBTI for various input data probabilities in a TG-MSFF. The value of T_{ff} is calculated using both the methods (5% increase in nominal T_{cq} and minimal D-Q point hereafter denoted as (1) and (2) respectively in all the figures marked) for the degraded design and the worst case T_{ff} can be computed. After 5 years, We clearly see that Low to High (LH) T_{ff} dominates the other as observed similarly in figure 5. Thus, deciding the values of T_{ff} from

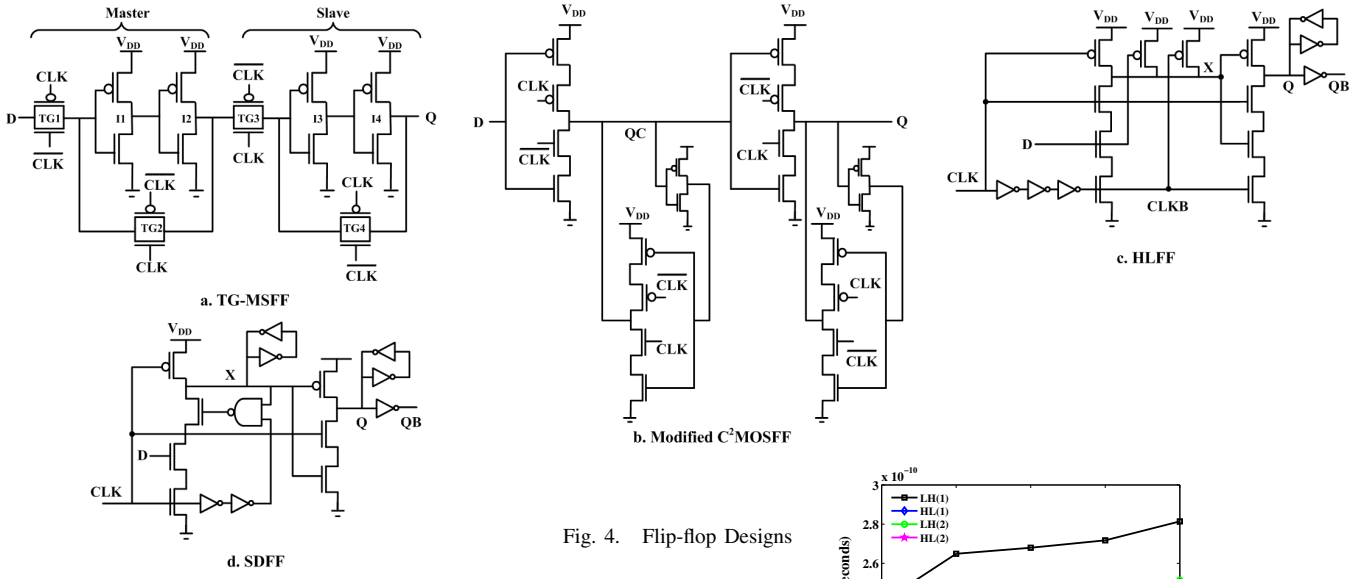

Fig. 4. Flip-flop Designs

this analysis will yield a fail proof design even after NBTI degradation. The points in Y axis on figure 7 indicate the values of T_{ff} of the unaged design.

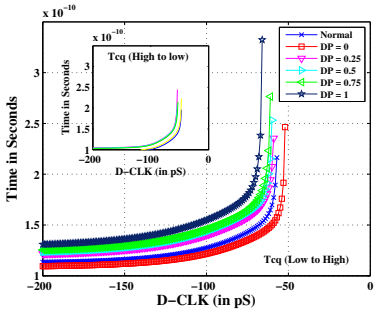

Fig. 5. Impact of input data probability on the timing characteristics of TG-MSFF

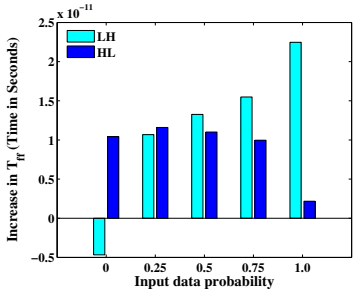

Fig. 6. Increase in T_{ff} with input data probability for a NBTI affected TG-MSFF

Modified C^{2}MOSFF shown in figure 4 (b) is more complex to analyze for the effect of NBTI. The setup time T_{su} and CLK-Q T_{cq} of modified C^{2}MOSFF is governed by the master and slave latches respectively similar to the TG-MSFF. From figure 8, we observe that T_{cq} of $0 \rightarrow 1$ transitions increase as the circuit undergoes aging. Figure 9 shows the increase in T_{ff} of a NBTI affected flip-flop if the signal arrives at the setup time (case 1) decided for the unaged flip-flop for both the transitions. This proves that the flip-flop is highly stressed if the input data remains at '1' most of the time. We observe that the T_{ff} which was dominant for $1 \rightarrow 0$ transitions (denoted as HL) change to $0 \rightarrow 1$ (denoted as

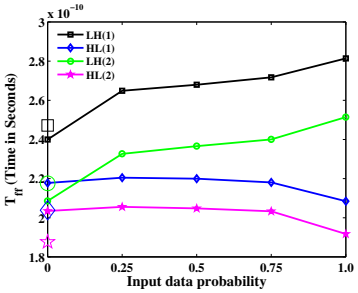

Fig. 7. Variation of optimal T_{ff} with input data probability for NBTI affected TG-MSFF

LH) at the end of stress period. Thus, it is imperative to study the impact of input data probability to calculate the worst case degradation when the effect of NBTI is analyzed. Figure 10 shows the analysis for deciding the value of T_{ff} in equation 3 after degradation due to NBTI for various input data probabilities in a C^{2}MOSFF. The nominal T_{ff} of an unaged design is shown on the Y axis. The points in Y axis on figure 7 indicate the values of T_{ff} of the unaged design. The hold time is still negative for C^{2}MOSFF and is not presented here.

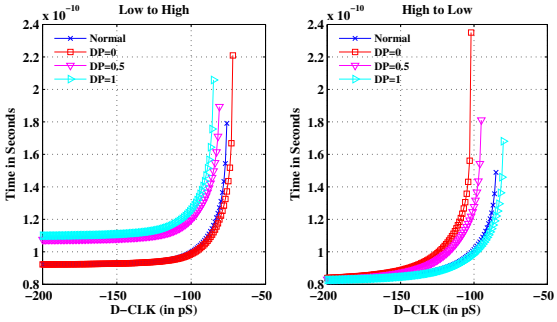

Fig. 8. Impact of input data probability on the timing characteristics of C^{2}MOSFF

B. Pulse Triggered Latches

Hybrid latch flip-flop (HLFF) which is a high performance storage element with very small delay. The data is latched during the transparency period created by the 1-1 overlap of CLK and CLKB shown in figure 4 (c). Odd number of inverters are inserted after the CLK signal to achieve CLKB. HLFF exhibits negative setup time and positive hold time. So, the data is allowed to arrive even after the clock edge and

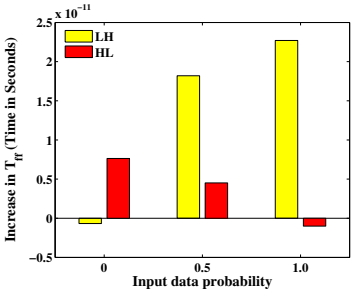

Fig. 9. Increase in T_{ff} with input data probability for a NBTI affected C^{2}MOSFF

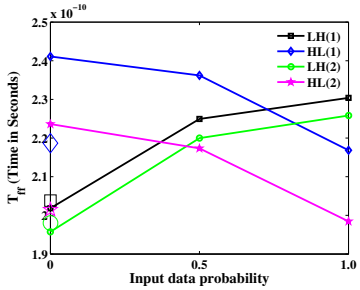

Fig. 10. Variation of optimal T_{ff} with input data probability for a NBTI affected C^{2}MOSFF

still be latched correctly. The hold time constraint is created by the falling edge of CLKB. Negative setup time helps in high speed circuit designs for slack borrowing, slack passing and absorption of clock skew. Positive hold time posts a negative impact on the circuit. Narrow transparency periods are advantageous because they reduce potential race through problems and increase immunity to noise. However, they should be long enough for the flip-flop to latch on correctly and to utilize the slack allowed for the data.

Figure 11 shows the increase in T_{ff} of a NBTI affected circuit for the zero setup time. It is obvious that the change in HLFF is negligible while SDFF shows a minimal increase than HLFF. As shown in figure 12 and 13, the variation of T_{ff} with the input data even after 5 years is minimal compared to master-slave latches. This is due to the basic topology of the circuits. The $0 \rightarrow 1$ transitions in pulsed latches depend on the strength of the NMOS stack of the pulse trigger circuit and the final PMOS transistor. In the case of HLFF, the intermediate node X is precharged to '1' (except the negligible time of discharge) and put the PMOS transistor in recovery mode. During the evaluate phase, it discharges to '0' if the input data is '1'. This causes the T_{cq} of HLFF to be almost constant thereby not degrading the performance (infact, slightly faster as the pull up PMOS in the pulse generator stage gets weakened). In the case of SDFF, the node X discharges only if the input D='0' and remains at the stress mode only for half of the clock cycle (it becomes a '1' at the precharge portion of the clock cycle). Therefore, the T_{cq} variation is SDFF is also minimal ($\sim$4ps). The variation in figure 13 reflects this change in the stress of the PMOS according to the data rate. However, this is also minimal compared to master-slave latches. The points in Y axis on figures 12 and 13 indicate the values of T_{ff} of the unaged design.

The transparency period play a critical role and should be long enough for the correct pulse to get latched while it imposes a longer hold time if it is large. NBTI causes an increase in the delay through the buffers and therefore increases the width of the transparency region. Table I shows the increase in the transparency widths of HLFF and SDFF over a period of 5 years with the duty cycle of clock being 50%. The increase in delay is due to the increase in the threshold of the second inverter in the buffer section of the pulse generator which results in a longer $0 \rightarrow 1$ transition while the first and third in HLFF undergo a $1 \rightarrow 0$ transition (the third inverter in SDFF is replaced by a NAND gate as shown in the figure 4(d)). The NAND gate also undergoes aging depending on the input data and plays a role in the conditional shut off time. The hold time for these pulsed latches are generally taken as the width of the transparency regions and as shown in table I, it shows a minimal increase ($\sim$4ps). This can be easily compensated by using buffer pads used for minimal combinational logic delay between flip-flop stages when there is no logic between them.

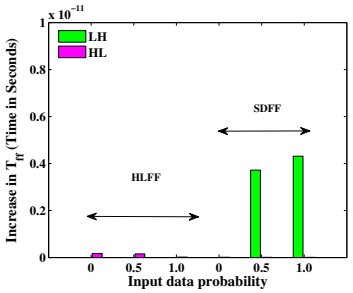

Fig. 11. Increase in T_{ff} with input data probability for a NBTI affected HLFF and SDFF

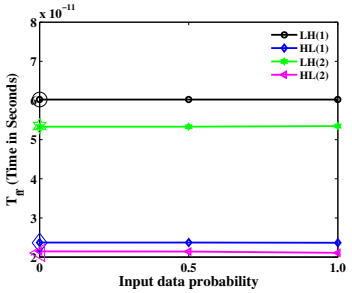

Fig. 12. Variation of optimal T_{ff} with input data probability for a NBTI affected HLFF

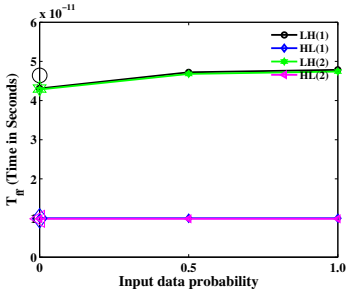

Fig. 13. Variation of optimal T_{ff} with input data probability for a NBTI affected SDFF

Figure 14 shows the nominal T_{cq} (average of both the transitions) of all the flip-flops. It is clear that the T_{cq} of TG-MSFF and C^{2}MOSFF are affected more while the HLFF undergoes the least degradation. SDFF on the other hand undergoes a much lesser degradation than the master-slave pairs, but more than HLFF due to the reasons explained in the earlier sections.

TABLE I

TRANSPARENCY PULSE-WIDTHS OF PULSE TRIGGERED LATCHES AFTER 5 YEARS

Flip-Flop	Normal (in pS)	NBTI affected (in pS)
HLFF	68.1	72.7
SDFF	35.0	38.2

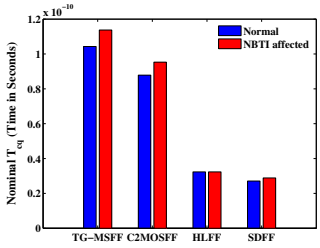

Fig. 14. Comparison of Normal and NBTI affected nominal T_{cq} for various flip-flops

Figure 15 shows the impact of temperature on NBTI on flip-flops. The impact of NBTI is dependent on the operation temperature as the change in threshold (ΔV_{th}) is exponentially dependent on temperature in the constant K_v in equation 1 and increases as temperature increases. The percentage degradation values of T_{ff} shown in figure 15 for three different temperatures were normalized to their base values at the same temperature. Higher temperatures cause higher percentage increase in the delays with master slave latches showing more degradation than pulse triggered latches. The absolute increase in the $0 \rightarrow 1$ transition in SDFF is still extremely small though the percentage degradation is higher as they are normalized to the base values.

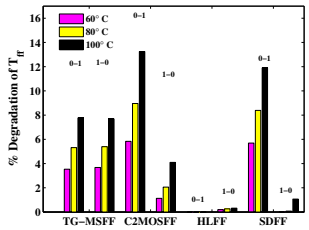

Fig. 15. Effect of temperature on NBTI degradation of flip-flops

Figure 16 shows the percentage variation of T_{ff} for various technologies at 80° for the input data probability of 0.5 (for realistic purposes) and at the setup time decided by case 1 for an unaged flip-flop. They values are normalized for the nominal unaged design of the technology. The change in threshold (ΔV_{th}) for lower technologies are much higher than 65 nm and the reduction in supply voltage augments the increase in the delays as shown in the figure. Even though, the percentage increase in delay for pulse triggered latches are high (SDFF 0-1), the absolute increase in delay from the nominal value is much smaller than the master slave latches.

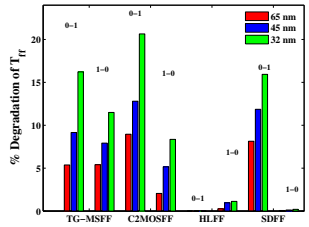

Fig. 16. Effect of NBTI on different technology nodes

V. CONCLUSION

In this paper, we have analyzed the impact of NBTI on the timing metrics of clocked storage elements. We show the impact of input data probability to analyze the worst case degradation conditions. We observe that master-slave latch pairs are affected more compared to pulse triggered latches. We also analyzed the impact of temperature on NBTI and the resulting degradation in the timing characteristics. The impact of NBTI on flip-flops of future technology nodes is also analyzed.

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