

Test Cost Minimization through Adaptive Test Development

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Abstract—The ever-increasing complexity of mixed-signal circuits imposes an increasingly complicated and comprehensive parametric test requirement, resulting in a highly lengthened manufacturing test phase. Attaining parametric test cost reduction with no test quality degradation constitutes a critical challenge during test development. The capability of parametric test data to capture systematic process variations engenders a highly accurate prediction of the efficiency of each test for a particular lot of chips even on the basis of a small quantity of characterized data. The predicted test efficiency further enables the adjustment of the test set and test order, leading to an early detection of faults. We explore such an adaptive strategy, by introducing a technique that prunes the test set based on a test correlation analysis. A test selection algorithm is proposed to identify the minimum set of tests that delivers a satisfactory defect coverage. A probabilistic measure that reflects the defect detection efficiency is used to order the test set so as to enhance the probability of an early detection of faulty chips. The test sequence is further optimized during the testing process by dynamically adjusting the initial test order to adapt to the local defect pattern fluctuations in the lot of chips under test. Experimental results show that the proposed technique delivers significant test time reductions while attaining higher test quality compared to previous adaptive test methodologies.

I. INTRODUCTION

Aggressive device scaling and integration keeps reducing chip manufacturing cost, yet with no diminution in sight for test cost. The end result is a significant magnification of the fraction accorded to test as part of the overall chip design and manufacturing cost. Test cost reduction has become a crucial issue in product development as it increasingly correlates with the overall cost control of the product.

Parametric test cost is one of the major bottlenecks for test cost reduction due to the relatively slow speeds of parametric testers and the highly diversified parameter types. Traditional parametric test methodologies fail to capture the impact of systematic process variations on the efficiency of distinct tests, thus restricting their ability to deliver significant test cost reductions. It has been widely observed that these systematic variations result in a non-uniform defect occurrence probability, leading to a highly skewed defect detection probability of the tests[2], [3]. Such an observation suggests a more desirable quality trade-off which enables an appreciable test cost reduction by applying a reduced set of tests while accepting a small number of faulty chip escapes[2], [3]. This trade-off can also be seen from a test economics perspective by analyzing the most recent industrial test cost data. It has been reported that test cost as a function of DPM improvement increases exponentially, whereas reductions in

shipping defect costs are sharply attenuated once certain low levels of DPM have been reached [1]. Therefore, for consumer electronics, it is cost-wise highly efficient to apply a reduced parametric test set while controlling the shipping defect cost to an acceptable level.

Test quality of a reduced parametric test set is highly dependent on its capability to target the defects that actually exist in chips under test. Information about defects in each lot of chips can deliver almost complete defect coverage when they are used to guide the selection of the most appropriate reduced test set. Since different lots of the same product might display significant variance as a result of process migration in predominating defect patterns, the reduced test set should not be rigidly cast even though the chips being tested are structurally identical. An adaptive identification of the reduced test set is needed for capturing the particularity of each individual lot. In addition to the use of a reduced test set, further test cost reduction can be attained by an appropriate ordering of tests during the test application for each individual chip. By arranging the tests that have higher defect detection probabilities in early positions in the test sequence, the test time for faulty chips can be significantly reduced since most ATE's operate in a stop-on-first-failure mode. The test order needs to be dynamically adjusted during testing to adapt to the fluctuation of defect patterns.

Such test identification and reordering schemes necessitate prediction of the fault detection efficiency of each test for a lot of chips. Thus the data already generated by the tester need to be effectively utilized to provide statistical information for future test guidance. One important feature that can be exploited is the correlation between parametric tests. To wit, a resistive open or short defect may yield highly consistent syndromes in test performance (the measured value of the parameter-under-test) of DC current and voltage tests. Since strongly correlated tests are highly likely to result in consistent test conclusions, most chips can be correctly tested as long as the best representative test within the group of correlated tests is added onto the test set. In case the representative test fails to cover the tests correlated with it, faulty chips may escape despite the testing and be shipped. However, if the probability of escapes is low enough, the benefit in test cost reduction outweighs the shipping defect cost.

Several initial applications of adaptive testing in industry have been reported in the literature. The work in [2] performs a lot-based characterization and selects the test set for each

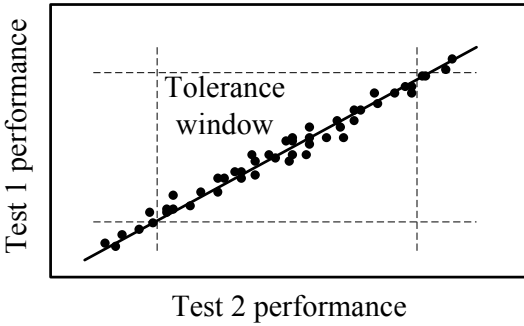


Fig. 1. Correlated test results

lot based on the distribution shape of the characterized data. An adaptive test ordering technique based on the failure counts of each vector is proposed in [3]. Adaptive techniques have also been applied to other test-related issues, such as path selection for delay test [4], diagnosis [5], IDDQ test [6] and SOC test scheduling [7]. Although appreciable benefits have already been observed in established work, no algorithmic approach has been proposed to efficiently utilize the correlation information in adaptive test development, hindering the full exploitation of the potential of adaptive techniques.

In this paper, we propose a two-stage adaptive test methodology for parametric test, one of the most expensive test phases. The first stage focuses on the generation of an appropriate reduced test set under the guidance of a correlation analysis. A graph model is developed to represent the correlation relationship among the candidate tests, based on which an algorithm is proposed to generate the minimum test set that covers all the correlated tests. The reduced test set is then ordered in the second stage using statistical models to maximize the overall probability of early fault detection. In order to respond to the impact of local defect pattern fluctuation on test order efficiency, this initial order is locally adjusted during the test application of each individual chip so as to attain further test time reduction.

Section II presents a set of motivating points for the proposed technique. The identification of the reduced test set is discussed in Section III. The test reordering technique for early detection of faulty chips is presented in Section IV. Section V discusses the issue of achieving a flexible application of the proposed technique based on the systematic defect pattern of the targeted fabrication process. The experimental results and comparisons with previous techniques are presented in Section VI. A brief set of conclusions is provided in Section VII.

II. MOTIVATION

A. Test set size reduction

The size of the applied test set determines test cost. While in the case of a good chip, the test cost of applying the full set of tests needs to be incurred, the case of a bad die introduces opportunities for test cost reduction as only the test time up to and including the application of the first test

that detects the defect needs to be incurred, in a stop-on-first-failure mode of testing. The defect probability distribution in chips is usually non-uniform due to the impact of systematic technology variations. As a result, several tests may have little or even no chance to detect any failure chip in the lot-under-test because the occurrence probability of the defects targeted by them is very low. If the prioritization of the defect detection probability of each test can be attained from the characterization of a small set of sampling test data, test time can be reduced by dropping the tests with the least criticality.

In addition to the dropping of tests with low fault detection probability, another level of test set size reduction can be achieved by utilizing the correlation between tests. The scattergram in Figure 1 illustrates the performance of two highly correlated tests. It can be seen that if one of these tests indicates that a chip is defect-free (the corresponding parameter is within the tolerance window), the other test with quite high likelihood would yield the same conclusion as well. The high concordance between the test conclusions of the two tests can also be observed in the converse case of a defective chip. Such a set of observations introduces the possibility of dropping one of the tests from the pair. While the test cost implications of such an opportunity may be significant, the impact on test quality may be limited as the defects the dropped test detects may quite likely be detected by the alternative test. While in this small example, either test could be dropped with no adverse consequence, more complex, realistic correlation cases may necessitate careful test set pruning process guided by an appropriate correlation model.

B. Search for the optimal test order

Although the test time for a good die is fixed no matter what order is used for applying the tests, the test time for a faulty die may vary greatly for distinct test orders. A demonstrative example reported in [3] shows that an appreciable test time improvement can be expected if the ideal test order is known *a priori*. The approximation of the ideal test order represents essentially a search for maximization of the early defect detection probability. Attaining such a goal requires mathematical models that predict the capability of a particular test in detecting the defects that have not yet been covered by the tests before it, in turn again necessitating an accurate correlation analysis between tests.

Considering that the systematic variation may fluctuate gradually in a sequence of chips, the globally optimal test order can be further improved by performing local adjustments on-line. This requires the development of a set of cost-effective adjustment heuristics that can be quickly computed on the fly based on the test data collected from the subsequence of chips tested most recently.

III. MINIMUM TEST SET IDENTIFICATION

The pruning of the test set is performed by analyzing the statistical features of the characterized data obtained by applying the full test to a small number of sample chips.

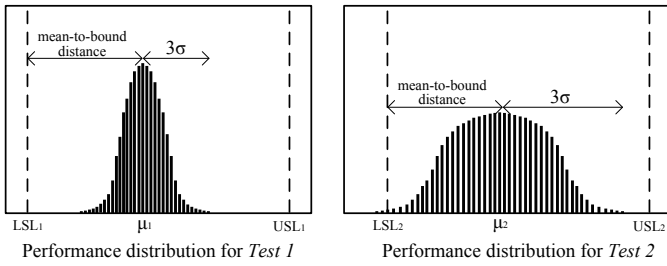


Fig. 2. Test dropping based on Cpk

The reduced test set needs to be updated from lot-to-lot to account for fabrication process migration.

A. Preprocessing phase

The complete set of tests is applied to a small set of randomly selected sample chips and the test results are collected. A performance distribution can be constructed for each test and the correlation coefficient between each pair of tests can also be extracted from the sampled data.

Because of the non-uniform defect pattern in the lot under test, the performance distributions of distinct tests will exhibit highly varying statistical features. A test fails only when the observed performance falls out of the tolerance bound. If the distribution of a test is quite concentrated around the nominal point of the performance (i.e., far away from both the lower and upper bounds of the tolerance region), the probability of this test detecting any defects in the lot under test is low. Hence the defect detection probability of each individual test can be evaluated from its distribution, and the non-critical tests can be directly dropped from the test set with little impact on test quality. In our work, we continue to use the Cpk metric (Process Capability Index) [2] that is widely used in industrial characterization to prioritize the criticality of each test. The Cpk measures how successfully the process pushes the distribution far away from the specification limits. Mathematically, it is defined as the ratio of the distance between the mean and the closest limit to the 3σ spread of the distribution, as shown in the equation below.

$$Cpk = \min\left[\frac{USL - \mu}{3\sigma}, \frac{\mu - LSL}{3\sigma}\right] \quad (1)$$

where USL and LSL denote the upper and lower specification limits, respectively. A higher Cpk value denotes a reduced probability of the performance falling out of the acceptance region, thus resulting in a lower defect detection probability. As shown in Figure 2, the performance distribution for *Test 1* has a higher Cpk than that of *Test 2*, indicating that dropping *Test 1* has less impact on test quality than dropping *Test 2*. The determination of the Cpk threshold for test dropping depends on the targeted test quality. A threshold of 2 is conventionally suggested as it translates into a 6σ quality, believed to deliver an exceedingly low DPM while still providing significant potential for test dropping.

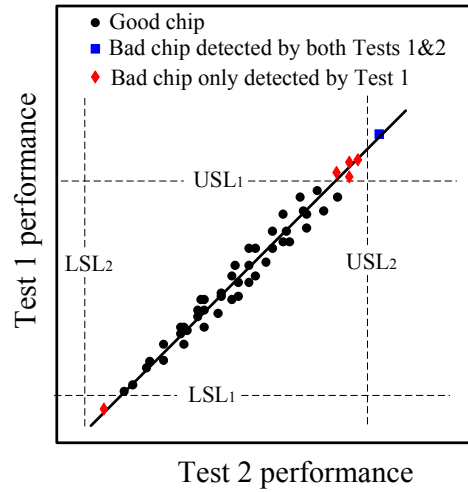


Fig. 3. Asymmetric impact of test dropping decisions on test quality

B. Dropping of correlated tests

After the individual test dropping in the preprocessing phase, the remaining tests are all critical if examined individually. Nonetheless, the correlation between tests provides further opportunities for test dropping, as outlined in Section II. The complicated correlation mechanism among the tests though imposes significant challenges for this test dropping phase.

One important issue that is highly critical to the overall test quality consists of the varying impact of distinct test dropping decisions for a pair of correlated tests. The defect detection capability of two tests may differ quite a bit even if they are highly correlated, resulting in an asymmetric test dropping impact. This effect is illustrated in the scattergram in Figure 3. Although a high correlation can be observed for the two tests shown in the figure, the distribution of *Test 1* contains more points that fall out of the acceptance region than *Test 2*, thus indicating a higher probability of the defects that escape *Test 2* being detected by *Test 1* than the converse situation. Such an asymmetric test quality implication can be reflected by the distinct Cpk values of correlated tests. More specifically, dropping the test with a higher Cpk value from a pair of correlated tests delivers a better test quality because of the higher probability of the defects targeted by the high-Cpk test being covered by the low-Cpk test.

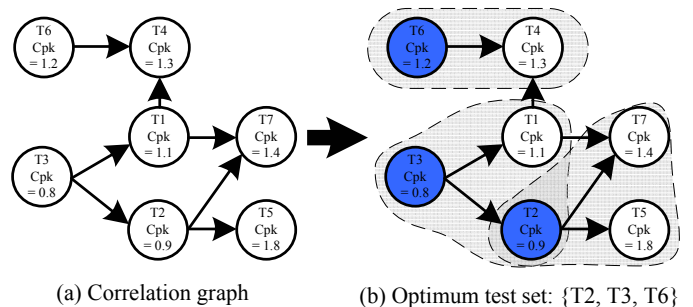


Fig. 4. Graph representation of correlations between tests

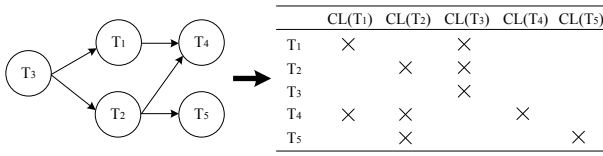


Fig. 5. Cover table construction

Taking into account the asymmetric impact of test dropping decisions discussed above, the correlation mechanism among the tests can be modeled by a directed acyclic graph as shown in Figure 4(a). Each test is represented by a vertex in the graph. A directed edge between two vertices denotes a correlation coefficient between the corresponding tests exceeding a certain threshold. The directed edge emanates from the low-Cpk test to the high-Cpk test, denoting the higher probability of the defects tested by the sink node being covered by the source node tests. In such a graph representation, if a certain vertex is selected in the test set, all its direct successors can be dropped with little impact on test quality. Therefore, if we construct for each test its corresponding cover list that consists of itself and its direct successors in the correlation graph, the problem of searching for the most appropriate test set maps to the identification of a minimum set of cover lists that cover all the vertices in the graph, as shown in Figure 4(b).

This problem can be resolved by applying a modified version of the Quine-McCluskey algorithm [8]. As shown in Figure 5, a cover table can be constructed based on the correlation graph. Each column in the table corresponds to the cover list of a test and each row to a test that needs to be covered. By selecting the minimum number of columns (cover lists) that covers all the rows (tests), the most appropriate test set can be obtained.

The concepts of essentiality, row dominance and column dominance employed in the Quine-McCluskey algorithm all apply to this cover problem. An essential cover list contains at least one test that is covered only by itself. Such a test must be added to the ultimate test set to guarantee a full coverage of the tests. The rows that are covered by an essential cover list can all be crossed out from the table once the corresponding essential test has been added to the test set. If one column is dominated by another column (i.e., the case that the list covered by one test is completely contained in the list covered by another test), the dominated column can be crossed out from the table because the dominating column covers all the tests that are covered by the dominated column. However, if one row is dominated by another row (i.e., the case that the set of tests that cover a particular test is completely contained in the set of tests that cover another test), the dominating row is crossed out from the table because the covering of the dominating row will be automatically resolved by the covering of the dominated row. Such a table manipulation process may generate a new essential test that must be incorporated in the ultimate test set. Therefore, the most appropriate test set can be selected by iteratively performing the table manipulations based on the essentiality and dominance relationships.

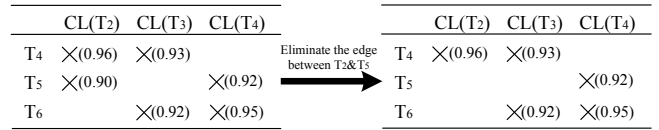


Fig. 6. "X" elimination for breaking cyclic situation

The cover table manipulation process may occasionally run into cyclic situations where neither the essentiality nor the dominance relationship is applicable. Such a situation constitutes the major challenge in Quine-McCluskey problems, necessitating a time-consuming branch-and-bound search. We avoid such a computationally expensive search process by utilizing a tie-breaker strategy that delivers test quality improvement. Since an "X" symbol in the table essentially denotes a high correlation between the pair of tests associated with the corresponding column and row, we can label it with the corresponding correlation coefficient value. Such a value can be used as a tie-breaker for handling a cyclic cover table as it reflects the capability of a test dropping decision in preserving test quality. As shown in Figure 6, whenever a cyclic situation is encountered, the "X" symbols with the least correlation value are eliminated from the table until a new essentiality or dominance relationship is generated. Eliminating an "X" symbol corresponds to excluding the choice of dropping tests based on the correlation denoted by that "X" symbol. The rationale for such a tie-breaker strategy can be seen in that a lower probability of test escape can be expected by forcing the test dropping process to concentrate on tests with higher correlations. Once a new essentiality or dominance relationship emerges, the table manipulation operations outlined can again be iteratively applied until all the rows have been covered by the selected tests.

IV. TEST REORDERING FOR EARLY FAULT DETECTION

As pinpointed in Section II, the non-uniform systematic defect distribution contributes to a skew in defect detection probabilities of the tests. Thus the chance of early detection of defective chips can be increased by appropriately adjusting the order of test application. The attainment of the optimal test order requires a good prediction of the defect patterns in the chips coming up for test. Traditional adaptive techniques usually resolve this problem by ordering tests according to the cumulative first-failure count of each test. Such a strategy fails to establish a global view on the effects of test order on test efficiency, as it relies on biased information about the first-failing tests collected from the dies already tested. We aim at avoiding this problem by investigating the global order implication at the beginning of the test process so that the entire testing process can benefit from the global information. We first construct based on the characterized data a statistical model to calculate the probability of each test detecting the defects that have not yet been covered by the preceding tests. Based on this statistical model an initial test order can be statically identified that maximizes the overall opportunity of early fault detection. This initial

order is used as a fundamental order throughout the entire testing process, and only local adjustments on it are allowed. During test application, the first-failure count of each test is collected only from dies that are most recently tested. This run-time information is used to dynamically adjust the fundamental order to adapt to the local fluctuation of defect patterns. Such a two-phase ordering strategy enables a more informed ordering decision due to a combined utilization of the global and local information.

A. Initial order determination

Since the testing results for the chips in the same lot are usually normally distributed [2], the corresponding probability density function (PDF) can be directly specified by the characterized data obtained in the preprocessing phase. The determination of the appropriate order necessitates the examination of the mutual relationship between tests as well. Thus we need to first investigate how the order between two tests impacts test efficiency and then extend it to the case of multiple tests. Let us consider two tests, namely T_1 and T_2 . The joint distribution of their test results can be modeled as a bivariate normal distribution $N(\mu_1, \mu_2, \sigma_1^2, \sigma_2^2, \rho)$, where the mean (μ), variance (σ^2) and correlation coefficient (ρ) have all been characterized in the preprocessing phase. Let $f(t_1, t_2)$ denote the PDF for this distribution, where t_1 and t_2 are random variables denoting the test results of T_1 and T_2 , respectively. If T_1 is applied before T_2 during the testing process, the probability of T_2 detecting any defects that are not covered by T_1 can be calculated as the probability of t_2 falling out of its tolerance window given that t_1 is within its tolerance window, as specified by the equation below.

$$P_{det}(T_2|T_1) = \int_{-\infty}^{LSL_2} \int_{LSL_1}^{USL_1} f(t_1, t_2) dt_1 dt_2 + \int_{USL_2}^{+\infty} \int_{LSL_1}^{USL_1} f(t_1, t_2) dt_1 dt_2 \quad (2)$$

This pairwise relationship can be used to estimate the defect detection probability of a test in an actual test sequence. For any test T_i that follows a test sequence TS , its defect detection probability can be estimated as

$$P_{det}(T_i|TS) = \prod_j P_{det}(T_i|T_j), \forall j, \text{ s.t. } T_j \in TS \quad (3)$$

Although this estimation model ignores higher order correlations among multiple tests for the sake of computational effectiveness, the dominant correlation mechanism, the pairwise correlation, is accurately preserved. Since for test ordering purposes we only need information about the relative magnitudes of the defect detection probabilities of distinct tests, the proposed estimation model is accurate enough to guide the test ordering process.

The aforementioned estimation model enables the arrangement of the tests in such an order that the probability of early defect detection is maximized. The choice of the first test is purely determined by the Cpk values. The one with the least Cpk value is selected as its sampling data exhibits the largest failure probability. The order of

subsequent tests is determined using the proposed estimation model by always placing the test with the highest defect detection probability in the earliest possible position. Every time a new test is placed into the test sequence, the defect detection probabilities of the remaining tests need to be updated before arranging the next test as the list of preceding tests has changed. Such a test ordering process is detailed in Algorithm 1.

Algorithm 1 Initial ordering of tests

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 $TS \leftarrow \emptyset$ 
 $U \leftarrow$  unordered test set
 $i \leftarrow 1$ 
The  $i^{th}$  position of  $TS \leftarrow$  the test with least Cpk; Remove the selected test from  $U$ .
while  $U \neq \emptyset$  do
   $i = i + 1$ 
  Update  $P_{det}(T_j|TS), \forall T_j \in U$ 
  The  $i^{th}$  position of  $TS \leftarrow T_k \in U, \text{ s.t. } P_{det}(T_k|TS) = \max\{P_{det}(T_j|TS)|T_j \in U\}$ ; Remove  $T_k$  from  $U$ .
end while

```

B. Run-time test order adjustment

The static ordering step discussed above concentrates on delivering a globally optimal initial order for the testing process. If we allow this fundamental order to be adaptively adjusted during testing, further test time reduction can be expected as the local fluctuation of the defect pattern might cause the locally optimal order to differ somewhat from the globally optimal one. However, such an adjustment must be constrained within a local level to avoid destroying the global optimality of the initial order. According to these principles, we propose to monitor the chips within a running window during the test process. When the testing process moves to the i^{th} chip in the lot, the running window consists of the N chips that are tested immediately before Chip i . The first-failure tests are recorded only for the chips within the running window because these data reflect the local fluctuation of the defect pattern. The tests that detect these first-failures are moved forward from their original positions in the initial order, and the new test sequence is used for testing Chip i . This adjustment is expected to deliver an earlier defect detection as the systematic process variation may result in the same group of defects in Chip i as in the chips within the running window. The magnitude of such a forward movement for a particular test is determined by the number of bad chips within the running window that have been detected by this test. More specifically, if a test, T , has detected the first-failures of m out of the N chips in the running window, it is moved forward to a new position specified by the heuristic defined in Equation (4).

$$Position_{new}(T) = (N - m)/N * Position_{init}(T) \quad (4)$$

This heuristic correlates the magnitude of test order adjustment with the confidence level regarding the defect detection capability of the tests. If no information about the local defect pattern can be obtained at some point during testing (i.e., in

case all the chips in the running window are defect-free), no adjustment will be performed by the proposed heuristic, and the global test order (the initial order) will be retained. The low computational overhead of the proposed heuristic favors its utilization in a high speed testing environment for online test reordering.

V. ACHIEVING A FLEXIBLE TECHNIQUE APPLICATION

If a certain level of knowledge about the systematic defect behavior is known for the targeted fabrication technology, the proposed adaptive scheme can be applied in a more flexible manner than the strict lot-level test development strategy discussed above. For example, one common effect that has been observed for many fabrication techniques is that the edge and center areas of the wafer have a higher defect density than the remaining area [3]. This observation clearly shows that an evident skew exists between the defect patterns in different areas on the wafer. Hence we can group the dies from the same lot based on their locations on the wafer and apply the proposed adaptive scheme to each group individually. Larger test cost reduction and higher test quality can be expected in this more fine-grained application level because a more accurate characterization is thus possible. For fabrications that exhibit other types of systematic defect patterns, the granularity of the application level of the proposed methodology needs to be specified accordingly.

VI. EXPERIMENTAL RESULTS

The effectiveness of the proposed technique is evaluated by simulating the testing process. A set of 200 candidate parametric tests is assumed and their performance values on 10000 dies are generated. In line with the wafer characterization results reported in previous work [2], normal distributions are assumed for these performance data. 500 randomly selected dies are used for statistical feature characterization in the preprocessing phase. Adaptive test is applied to the remaining 9500 dies. The test simulation program is implemented in C and Matlab.

The proposed technique is compared with the conventional non-adaptive test scheme and the adaptive test technique proposed in [2] in terms of test cost (test time) and test quality (test escape quantity). The non-adaptive test is considered as the baseline approach as it incurs no test escape. The simulation results for the three techniques are listed in Table 1. Both the proposed technique and the adaptive approach proposed in [2] result in appreciable test time reduction at the cost of a small number of test escapes (the escape ratio is below 0.2%), thus confirming the effectiveness of adaptive schemes in test development. The last column

TABLE I
COMPARISON OF THREE TEST SCHEMES

Methods Results	Non-adaptive	Adaptive[2]	Proposed method	Improvement over [2]
Test time (sec.)	35812.92	29424.00	16029.06	45.5%
# test escape	0	20	16	20.0%

of the table shows the comparison between the proposed technique and the approach in [2]. Distinct benefits of the proposed technique over the previous adaptive approach can be observed, both in terms of test cost and quality. The improvement mainly stems from the optimal utilization of the correlation information in test dropping and reordering.

We have also examined the individual contribution of the test dropping and reordering strategy. If the reduced test set is applied without ordering, the improvement on test time reduces to 39.7%. It can be seen that the test dropping stage has a much larger contribution to test cost reduction than test reordering, as perhaps the test dropping stage excludes all non-critical tests, thus leaving a smaller optimization horizon for the subsequent ordering step. Nevertheless, the reordering technique is still valuable as it further improves the test cost by 5.8% with no impact on test quality.

VII. CONCLUSION

Test cost reduction plays an increasingly important role in the overall chip cost control as design and fabrication techniques advance. The idea of adaptive test has recently been incorporated into industrial applications for resolving the test cost problem. However, exploiting the full strength of adaptive test while maintaining satisfactory test quality necessitates an algorithmic level investigation of the underlying physical mechanisms such as systematic variation and test correlation. In this paper, we focus on examining the implication of test-to-test correlation on test set minimization, and propose an algorithm for generating the most appropriate test set based on a correlation graph model. An adaptive test reordering technique is also proposed to deliver an optimal application of the reduced test set identified in the first stage. The ordering strategy enables an early detection of faulty chips by superimposing a dynamically-performed local adjustment upon an optimal initial order that has been statically determined using a probabilistic defect detection model. Simulation results confirm that a high quality yet low cost testing process can be attained using the proposed methodology.

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