Timing Analysis Considering IR Drop Waveforms in Power Gating Designs

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***Abstract*—IR drop noise has become a critical issue in advanced process technologies. Traditionally, timing analysis in which the IR drop noise is considered assumes a worst-case IR drop for each gate; however, using this assumption provides unduly pessimistic results. In this paper, we describe a timing analysis approach for power gating designs. To improve the accuracy of the gate delay calculation we determine the virtual voltage level by taking into account the IR drop waveforms across the sleep transistors. These can be obtained efficiently using a linear programming approach. Our experimental results are very promising.**

I. INTRODUCTION

As the VLSI design process continues to scale down, the noise problem has become critical because it may degrade a circuit's performance and cause erroneous output values. Supply and reference voltage fluctuations are sources of IR drop noise. Traditionally, after the worst-case IR drop is determined, it is used by the timing analyzer to estimate a circuit's delay; however, using the worst-case IR drop can provide unnecessarily pessimistic results. Because IR drop depends on the applied input vectors, IR drop varies over time and is different for different nodes on the power grid. It is also well known that the worst cases of IR drop only occur occasionally.

There have been several previous works [1][3][5][11][14] that address timing analysis with IR drop noise. Researchers [1][14] consider the variations of both power and ground voltages. The authors of [5] calculate circuit delay with IR drop noise by modeling it as an effective output load. Researchers in [11] provide a pattern searching technique for producing the worst-case delay on the critical paths. The authors of [3] present a pattern-independent method to calculate a tight upper bound on the delay along the selected path with IR drop noise.

Unlike previous works that focus on the IR drop of a power grid network, we studied the IR drop effect in a power gating design [2][7][12][13][16][17] in which the IR drop problem is even more severe. Power gating is used extensively in portable devices for leakage power reduction. Since the *on* resistances of the sleep transistors are relatively larger than the resistances of wires, currents may flow through the sleep transistors and cause larger IR drops across sleep transistors in the active mode. Hence, analyzing the timing with IR drop is very important in the power gating designs.

In this paper, we propose to an efficient method to use the ***IR drop waveforms*** to capture the time-varying voltage level of the local power grid that is connected to the global power grid through the sleep transistors in a power gating design. The IR drop waveform of a node on the power grid indicates the maximum possible IR drop value for every time instant. Although the number of nodes on a power grid can be large, the number of required IR drop waveforms across sleep transistors is limited by the number of sleep transistors, which is much less than the number of nodes on the global power grid. This is common in most power gated architectures, such as a Distributed Sleep Transistor Network (DSTN) [12].

Our contributions are as follows. First, we propose a linear programming solution to estimate the IR drop waveform without running massive numbers of SPICE-like simulations. Second, most of the previous works consider IR drop with ***decoupling capacitances*** (or ***decaps***) only through circuit simulations. We show how to compute the upper bound of the IR drop considering the effects of decaps. Finally, we apply the concept of the sliced switching window [4][15] to the timing analysis that considers the IR drop noise. The result shows that using the IR drop waveform can provide 83% more accuracy than the traditional method

The remainder of this paper is organized as follows. Section II presents our method for IR drop waveform estimation. Section III discusses how to apply the IR drop waveform in the static timing analysis. Section IV shows the experimental results. Section V presents our conclusions.

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II. FAST IR DROP WAVEFORM ESTIMATION

In this section, we first review the basic architecture of power gating designs in Section II.A. Then, we present our efficient IR drop waveform estimation method for a power gating design without considering decaps in Section II.B. Next, in Section II.C, we extend this method to consider decaps. Finally, we propose an improved method with decaps in Section II.D.

A. Basic Architecture of a Power Gating Design

In this paper, we use the DSTN architecture of a power gating design, as shown in Figure 1(a). In the DSTN architecture, a circuit is decomposed into several clusters, and each cluster is connected to a sleep transistor. Then, all sleep transistors are connected together by virtual power lines. Since sleep transistors operate in the linear region during the active mode, they can be modeled as resistors. Figure 1(b) shows a resistance network model of the power gating design in Figure 1(a). R_{STi} is the resistance of a sleep transistor *STi*; R_V is the resistance of a segment of the virtual power line; I_{Ci} is the current flowing through a cluster *Ci*; and I_{STi} denotes the current through a sleep transistor *STi*. Let us focus on the current through sleep transistor *ST3*, I_{ST3}, which is contributed by the currents I_{C1}, I_{C2}, and I_{C3} from all clusters. Using Kirchhoff's Current Law and Ohm's Law, the relationship between I_{STi} and I_{Ci} can be stated in matrix form as follows.

$$\begin{bmatrix} I_{ST1} \\ I_{ST2} \\ I_{ST3} \end{bmatrix} = \begin{bmatrix} r_{11} & r_{12} & r_{13} \\ r_{21} & r_{22} & r_{23} \\ r_{31} & r_{32} & r_{33} \end{bmatrix} \cdot \begin{bmatrix} I_{C1} \\ I_{C2} \\ I_{C3} \end{bmatrix} \qquad \text{EQ(1)}$$

where r_{ij}s are all constants. Let us take r_{11} as an example.

$$r_{11} = \frac{(R_V + R_{ST3}) \times R_{ST2} + R_V \times (R_V + R_{ST2} + R_{ST2})}{(R_V + R_{ST3}) \times R_{ST2} + (R_V + R_{ST1}) \times (R_V + R_{ST2} + R_{ST2})}$$

Using EQ(1), we can compute the current through a sleep transistor for a given pair of input vectors. First, for each pair of input patterns, we can obtain the current profile of clusters. With these, we can then derive the current profile through the sleep transistor by using EQ(1). Among all possible input patterns, we can find the ***maximum current*** through the sleep transistor *STi*, denoted as $\boldsymbol{MC_{STi}(t)}$ for a time instant *t*. Knowing the maximum current $MC_{STi}(t)$, we can then easily find the ***maximum IR drop*** $MIR_{STi}(t)$ using EQ(2).

$$MIR_{STi}(t) = MC_{STi}(t) \times R_{STi} \qquad \text{EQ(2)}$$

However, the process of determining $MC_{STi}(t)$ generally

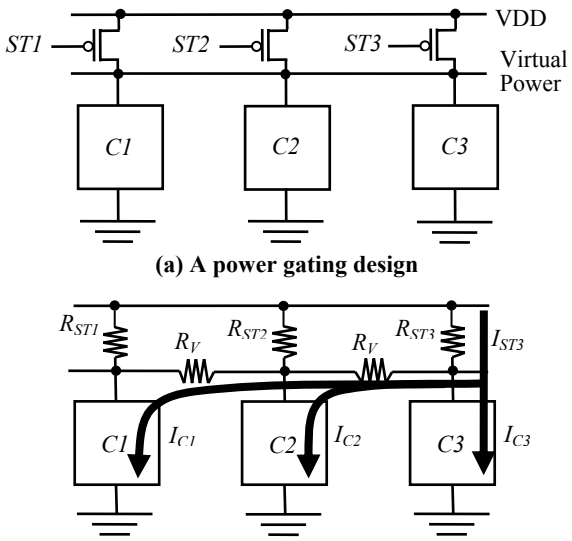

Figure 1: A power gating design with its corresponding resistance network

requires a massive number of circuit-level simulations. The process becomes impractical even for a medium-sized design. Although $MC_{STi}(t)$ is difficult to calculate, the ***maximum current*** of a cluster *Ci*, defined as $\boldsymbol{MC_{Ci}(t)}$, is quite easy to obtain. Many efficient methods have been proposed in [6][8][9][10]. In addition, CAD tools such as PrimePower™ are available, which enable us to perform a massive number of gate-level simulations to obtain the maximum current of a cluster.

In this paper, we assume that the maximum currents for the clusters are available. One simple way of estimating the maximum current through the sleep transistors, MC_{STi}, is to plug the maximum cluster current, MC_{Ci}, into its corresponding variable I_{Ci} in EQ(1). However, this simple estimation is unduly pessimistic because the maximum currents of different clusters usually do not occur simultaneously.

B. IR Drop Waveform Estimation without Decaps

Now, we formally formulate the problem of deriving IR drop waveforms for all nodes on the virtual power grid as shown in Figure 2. The input is a resistive network that models the sleep transistors and wire segments of the virtual power line. In addition, we assume that the waveforms of the clusters' maximum currents are available. Our objective is to find an accurate estimation of the sleep transistors' IR drop waveforms.

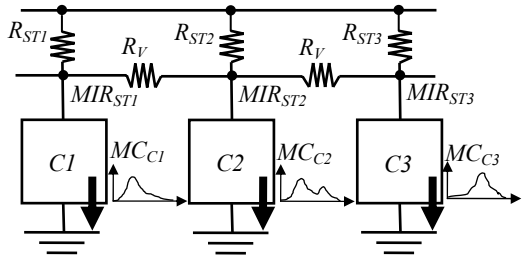

Figure 2: The IR drop waveform derivation for a resistance network

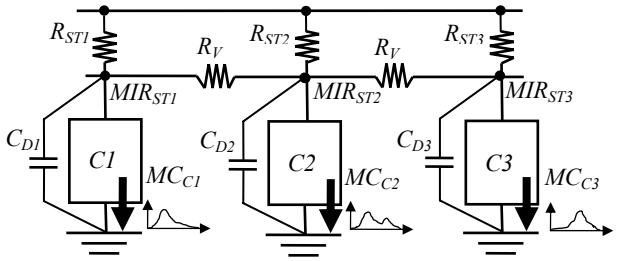

Figure 3: The IR drop waveform derivation for a resistance and capacitance network

We have noted that the maximum currents of different clusters usually do not occur at the same time; however, the maximum current for a cluster, $MC_{Ci}(t)$, can only be used to constrain the value of the corresponding I_{Ci}. For the correlation between different clusters, we can use the maximum current of different combinations of clusters to constrain the current through the corresponding clusters. For example, we can obtain $MC_{C1,C2}(t)$, which is the maximum current of the two clusters: *C1* and *C2*. With $MC_{C1,C2}(t)$, we must have $I_{C1} + I_{C2} \le MC_{C1,C2}(t)$. Our idea is to use such maximum currents as linear constraints to consider the correlations between different clusters and also to obtain $MIR_{STi}(t)$ by maximizing the value of IR_{STi}, which is the IR drop across the sleep transistor *STi*. Taking R_{ST1} in Figure 2 as an example, the linear program to find the $MIR_{ST1}(t)$ for a time instant t can be stated as follows:

Maximize

$$IR_{ST1} = \left(\sum_{i=1}^{3} I_{Ci} \cdot r_{1i} \right) \cdot R_{ST1} \qquad \text{EQ(3)}$$

Subject to

$$I_{Ci} \le MC_{Ci}(t) \quad \text{for } i = 1, 2, 3.$$
$$I_{C1} + I_{C2} \le MC_{C1,C2}(t)$$
$$I_{C1} + I_{C3} \le MC_{C1,C3}(t)$$
$$I_{C2} + I_{C3} \le MC_{C2,C3}(t)$$
$$I_{C1} + I_{C2} + I_{C3} \le MC_{C1,C2,C3}(t)$$

where r_{11}, r_{12}, and r_{13} are constants. The linear programming solution can efficiently find the waveform of MIR_{STi} and take into account that the maximum currents for the clusters do not occur simultaneously.

C. IR Drop Waveform Estimation with Decaps

Since decaps are commonly inserted between the ground and virtual power lines in a power gating design to prevent a sudden fluctuation of IR drops and to reduce the IR drop noise, it is important to consider their effect. In the previous section, we modeled the sleep transistor network as a linear system without considering decaps. In this section, we discuss how to modify the linear programming model to consider the effect of decaps. The circuit used for this problem is shown in Figure 3. Here, C_{Di} represents the capacitance of a decap *Di*. Again, we assume that the current profiles of all clusters are available.

With decaps, the value of the IR drop across a sleep transistor depends not only on the current flowing through the sleep transistor, but also on the previous voltages across decaps. Because of this dependency, the linear programming solution in EQ(3) cannot be directly applied. Since our objective is to find the maximum IR drop, we need to know which voltages on decaps at the previous time instant will cause the maximum IR drop at the current time instant. Luckily, we have the following lemma.

Lemma 1: In our linear programming model, the largest possible value of the IR drop occurs when all decaps at the previous time instant have the largest voltage values.

Proof: By using Kirchhoff's Current Law, the current through the sleep transistor *ST1* can be written as follows.

$$\frac{V_{ST1}(t)}{R_{ST1}} = I_{C1}(t) + \frac{V_{ST2}(t) - V_{ST1}(t)}{R_V} - V'_{ST1}(t) \cdot C_{D1} \qquad \text{EQ(4)}$$

Applying the Backward Euler technique with a fixed time step h, EQ(4) can be re-written as EQ(5), where $V_{ST1}(t\text{-}h)$ is the voltage across *ST1* at time instant *t-h*.

$$\frac{V_{ST1}(t)}{R_{ST1}} \cdot \left(\frac{h + R_{ST1} \cdot C_{D1}}{h} \right) = \left(I_{C1}(t) + \frac{V_{ST1}(t-h) \cdot C_{D1}}{h} \right) + \frac{V_{ST2}(t) - V_{ST1}(t)}{R_V} \qquad \text{EQ(5)}$$

Similarly, we can obtain the EQ(5) for *ST2* and *ST3*. Then we have the following matrix form.

$$\begin{bmatrix} \frac{V_{ST1}(t)}{R_{ST1}} \\ \frac{V_{ST2}(t)}{R_{ST2}} \\ \frac{V_{ST3}(t)}{R_{ST3}} \end{bmatrix} = \begin{bmatrix} \frac{h \cdot r_{11}}{h + R_{ST1} \cdot C_{D1}} & \frac{h \cdot r_{12}}{h + R_{ST1} \cdot C_{D1}} & \frac{h \cdot r_{13}}{h + R_{ST1} \cdot C_{D1}} \\ \frac{h \cdot r_{21}}{h + R_{ST2} \cdot C_{D2}} & \frac{h \cdot r_{22}}{h + R_{ST2} \cdot C_{D2}} & \frac{h \cdot r_{23}}{h + R_{ST2} \cdot C_{D2}} \\ \frac{h \cdot r_{31}}{h + R_{ST3} \cdot C_{D3}} & \frac{h \cdot r_{32}}{h + R_{ST3} \cdot C_{D3}} & \frac{h \cdot r_{33}}{h + R_{ST3} \cdot C_{D3}} \end{bmatrix} \cdot \begin{bmatrix} I_{C1}(t) + \frac{V_{ST1}(t-h) \cdot C_{D1}}{h} \\ I_{C2}(t) + \frac{V_{ST2}(t-h) \cdot C_{D2}}{h} \\ I_{C3}(t) + \frac{V_{ST3}(t-h) \cdot C_{D3}}{h} \end{bmatrix} \qquad \text{EQ(6)}$$

In EQ(6), the r_{ij}, C_{Di} , and R_{STi} are all positive constants. Therefore, in order for $V_{STi}(t)$ to have the maximum value, all $V_{STi}(t\text{-}h)$ must have the maximum value. Since decap stores the previous values, all decaps at the previous time instant must have the largest voltage values. Q.E.D

According to Lemma 1, if we have the largest voltages for all decaps at time instant $t\text{-}h$, $MIR_{STi}(t\text{-}h)$, we can obtain $MIR_{STi}(t)$ for all sleep transistors by using the linear programming method, but with many maximum currents of clusters as constraints. Using sleep transistor *ST1* in Figure 3 as an example, we can obtain $MIR_{ST1}(t)$ from the following formula.

Maximize

$$IR_{ST1}(t) = \left(\frac{R_{ST1}h}{h + R_{ST1}C_{D1}}\right)\left(\sum_{i=1}^{3} r_{1i} \cdot \left(I_{Ci}(t) + MIR_{ST1}(t-h)\left(\frac{C_{Di}}{h}\right)\right)\right) \quad \text{EQ(7)}$$

where the constraints are the same as in EQ(3). Furthermore, the voltage of decaps may not be zero at the initial time instant. To determine the value of $MIR_{STi}(0)$, we first consider $MIR_{STi}(0)$ as having a zero voltage level. Then, after deriving the IR drop waveform, we can obtain the value of $MIR_{STi}(T_{CYCLE})$ where T_{CYCLE} is the clock period. With the value of $MIR_{STi}(T_{CYCLE})$, we can assign $MIR_{STi}(0) = MIR_{STi}(T_{CYCLE})$ and derive a new IR drop waveform. We continue this step iteratively until the value of $MIR_{STi}(0)$ converges.

D. IR Drop Waveform Estimation with Decaps Considering Vector Correlation

To improve the accuracy of our IR drop estimation, we consider the correlation of decap voltage vectors. First, our estimation in the previous section is still pessimistic because the vector that induces MIR_{STi} at the previous time instant may not be the same as the vector that induces MIR_{STi} at the current time instant. In other words, the values of $MIR_{STi}(t\text{-}\triangle t)$ and $MIR_{STi}(t)$ may be affected by different vectors. The dependences that exist among decaps' values result in a conservative IR drop waveform calculation.

The maximum current of a cluster is obtained in our model by running a large input set of gate level simulations using PrimePower™. To reduce the correlation among the vectors, we partition all input vectors $\boldsymbol{V}$ into several partial sets such that $\boldsymbol{V} = \{V1, V2, V3 \ldots, Vn\}$. Thus, we can obtain the IR drop waveform for each set of vectors, $MIR_{STi}(t, Vk)$. Then, we obtain the IR drop waveform of the sleep transistor by finding the maximum value among $MIR_{STi}(t, Vk)$ at every time instant. Figure 4 shows the overall algorithm for the estimation of the IR drop waveform with decaps.

Algorithm IR_Waveform($MC_{Ci}(t)$, Ci, T_{CYCLE}, $\boldsymbol{V}$)
1. **foreach** Vk in set $\boldsymbol{V}$
2. **initial** $MIR_{STi}(0, Vk) = 0$ /*initial value of decaps as 0*/
3. **do**
4. **foreach** time instant t within T_{CYCLE}
5. find $MIR_{STi}(t, Vk)$ by linear programming
6. **end foreach**
7. $MIR_{STi}(0, Vk) = MIR_{STi}(T_{CYCLE}, Vk)$
8. **until** $MIR_{STi}(0, Vk)$ equals $MIR_{STi}(T_{CYCLE}, Vk)$
9. **end foreach**
10. $MIR_{STi}(t) = \text{Max}\{MIR_{STi}(t, Vk)\}$ for all t, k

Figure 4: Algorithm for IR drop waveform with decaps

III. TIMING ANALYSIS WITH IR DROP WAVEFORMS

Since IR drop will affect timing, in this section, we discuss how to perform the timing analysis to incorporate IR drop waveforms. We will use the sliced switching window. We define the gate's *switching window* as the time period between its earliest and latest arrival times. We divide the gate's switching windows into a set of small periods, called *slices*. The set of slices obtained for one gate is the *sliced switching window*.

With the IR drop waveform for a gate, we have information about the largest IR drop within each time slice. For example, in Figure 5, the largest IR drop within the slice [400, 500] is 0.082 V. For each slice in the switching window of a gate, we use its largest IR drop for computing the corresponding IR drop noise induced delay by applying the methods described in [1][14]. When the noise delays of all slices have been obtained, we can determine the gate's delay.

We use an example to illustrate the computation of the IR drop noise delay on a slice of a switching window. Suppose the IR drop waveform of a gate under consideration is as shown in Figure 5. Without considering the IR drop noise, the gate's switching window is [400, 700]. We divide the switching window of the gate into three slices {[400, 500], [500, 600], [600, 700]} of equal size: 100 ps. The largest IR drops of the gate are 0.082 V, 0.074 V, and 0.051 V within these three slices. For the first

slice [400, 500], we use the IR drop noise of 0.075 V to calculate the delay Δd_1. The first slice is then extended to be [400, 500+Δd_1] when considering the IR drop noise. Similarly, for the other two slices, we have [500, 600+Δd_2] and [600, 700+Δd_3]. In this example, suppose the maximum value among {500+Δd_1, 600+Δd_2, 700+Δd_3} is 600+Δd_2. Since the largest delay now is 600+Δd_2, the gate's switching window can be extended to [400, 600+Δd_2]. If we consider [400, 700] as a basic unit, the largest IR drop within the switching window is 0.082 V, which is less than the peak IR drop of 0.098V. Then, the switching window considering the IR drop noise will be [400, 700+Δd]; Δd is the noise delay under a 0.082 V IR drop. When we get the whole picture of the updated slices, we can easily obtain the delay for the entire circuit.

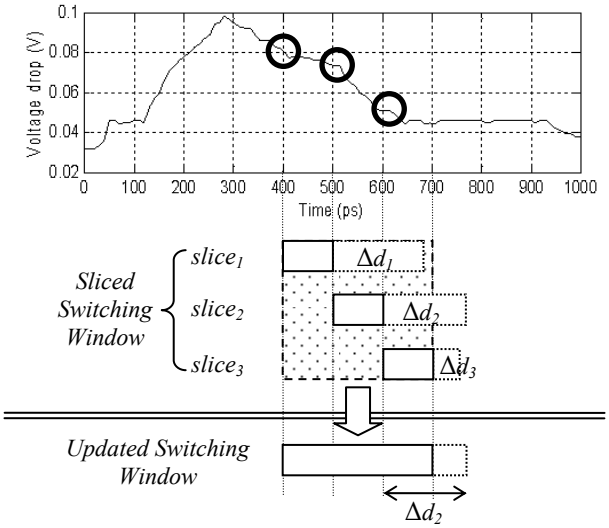

Figure 5: Noise delay computation with IR drop noise

IV. Experimental Results

We implemented the algorithms in Sections II and III and applied them to several benchmark circuits using the TSMC 90 nm CMOS technology process. These circuits were implemented using the power gating design style [2][7][12][13]. The implementation steps are shown in the following. First, a benchmark circuit is synthesized and placed. After that, we group the gates in the same row into a cluster that connects to a sleep transistor. The sleep transistors are inserted on the side of a row and underneath a power trunk. Decaps are placed near each sleep transistor and the value of a decap is assumed to be 0.5 pF. Then, we generated maximum current waveforms of clusters by using PrimePower™ with 10,000 random vectors.

In the TSMC 90 nm process, the on resistance of a 1μm sleep transistor is 2499 Ohm but the resistance of a 1μm Metal 1 wire is only 0.3 Ohm. The resistance of a wire is relatively small compared to the on resistance of a sleep transistor. Therefore, without losing much accuracy in the estimation, the IR drop of a node on the virtual power grid can be obtained from the IR drop of the node's corresponding sleep transistor.

Table 1 shows the results of our experiments. Column 1 shows the name of a benchmark circuit. Column 2 shows the number of sleep transistors. Column 3 shows a circuit's delay without IR drop noise. In an IR drop waveform, the peak IR drop denotes the largest value of the IR drop waveform. We use the peak IR drop as a constant for the whole cycle to pessimistically estimate the noise delay and report the noise delay, shown in Column 4. Note that the noise delay is the difference of a circuit's delay with noise minus a circuit's delay without noise. We then estimate a circuit's noise delay by using the IR drop waveform. The results are shown in Column 5. In columns 7 and 8, we show the circuit's noise delay considering decaps using the peak IR drop and using the IR drop waveform, respectively. Columns 6 and 9 show the runtimes for the IR drop timing analysis without and with decaps.

On average, compared to using the peak IR drop, noise delay over-estimation using IR drop waveforms can be reduced about 83%. The results show that our method, while still being pessimistic, can significantly increase the accuracy of the circuit delay estimation.

V. Conclusions

In this paper, we have proposed a novel algorithm to derive IR drop waveforms considering the effect of decaps for the power-gating designs. We applied the sliced switching window to IR drop waveforms in order to obtain accurate noise delays. On average, our algorithm can reduce noise delay over-estimation by about 83%.

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Table 1: The comparison between noise delays

Name	ST #	Circuit delay w/o noise (ns)	Noise delay without decaps (ns)		Runtime (Sec.)	Noise delay with decaps (ns)		Runtime (Sec.)
			Peak IR drop	IR drop wavefom		Peak IR drop	IR drop waveform	
C880	15	0.815	0.145	0.075	2.07	0.033	0.019	5.67
C6288	48	1.102	0.169	0.139	67.50	0.095	0.048	72.00
C7552	43	1.807	0.185	0.096	27.94	0.065	0.053	28.84
C3540	26	1.098	0.138	0.079	9.05	0.040	0.026	18.95
C5315	33	0.776	0.175	0.062	9.75	0.042	0.027	22.35
C1355	18	0.849	0.158	0.083	4.14	0.019	0.015	9.54
C432	10	0.470	0.163	0.069	1.10	0.020	0.014	3.80
dalu	21	0.607	0.102	0.047	2.50	0.017	0.010	7.00
i4	11	0.505	0.116	0.027	0.42	0.027	0.012	2.22
i5	9	0.419	0.084	0.032	0.35	0.021	0.014	1.25
i8	19	0.474	0.108	0.047	3.18	0.052	0.044	9.48
alu4	21	0.937	0.174	0.080	6.07	0.028	0.014	15.97
AVG			1	0.487		0.267	0.173	

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