Imperfection-Immune Carbon Nanotube Digital VLSI

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Abstract

Carbon Nanotube Field Effect Transistors (CNFETs), consisting of semiconducting single-walled Carbon Nanotubes (CNTs), show great promise as extensions to silicon CMOS and in large-area electronics. While there has been significant progress at a single-device level, a major gap exists between such results and their transformation into VLSI CNFET technologies. Major CNFET technology challenges include mis-positioned CNTs, metallic CNTs, and wafer-scale processing. We present design and processing techniques to overcome these challenges. Experimental results demonstrate the effectiveness of the presented techniques.

Mis-positioned CNTs can result in incorrect logic functionality of CNFET circuits. A new layout design technique produces CNFET circuits for arbitrary logic functions that are immune to a large number of mis-positioned CNTs. This technique is significantly more efficient compared to traditional defect- and fault-tolerance. Furthermore, it is VLSI-compatible and does not require changes to existing VLSI design and manufacturing flows.

A CNT can be semiconducting or metallic depending upon the arrangement of carbon atoms. Typical CNT synthesis techniques yield ~33% metallic CNTs. Metallic CNTs create source-drain shorts in CNFETs resulting in excessive leakage ($I_{on}/I_{off} < 5$) and highly degraded noise margins. We will present VLSI-compatible techniques for mitigating metallic CNT challenges. These techniques produce CNFET circuits with I_{on}/I_{off} in the range of 10^3-10^5, and overcome the limitations of existing metallic-CNT removal techniques.

The above techniques are demonstrated for complex logic structures using wafer-scale growth of (99.5%) aligned CNTs on single-crystal quartz and wafer-scale CNT transfer from quartz to silicon. Such an integrated approach enables experimental demonstration of cascaded CNFET logic circuits.