# 3D Stacked Power Distribution Considering Substrate Coupling

Amirali Shayan, Xiang Hu
Wanping Zhang, Chung-Kuan Cheng
*University of California, San Diego*
{*amirali,x2hu,w7zhang,ckcheng*}*@ucsd.edu*

A. Ege Engin
*San Diego State University*
*aengin@mail.sdsu.edu*

Xiaoming Chen
Mikhail Popovich
*Qualcomm, Inc.*
{*mikhailp,xiaoming*}*@qualcomm.com*

***Abstract*— Reliable design of power distribution network for stacked integrated circuits introduces new challenges i.e., substrate coupling among through silicon vias (TSVs) and tiers grid in addition to reliability issues such as electromigration and thermo-mechanical stress, compared to conventional System on Chip (SoC). In this paper a comprehensive modeling of the TSV and stacked power grid with frequency dependent parasitic is proposed. The analytical model considers the impact of the substrate coupling between the TSVs and layers grid. A frequency domain based analysis flow is introduced to incorporate frequency dependent parasitics. The design of a reliable power distribution network is formulated as an optimization problem to minimize power noise under reliability and electro-migration constraints. Experimental results demonstrate the efficacy of the problem formulation and solution technique.**

## I. Introduction

Three dimensional integrated circuits introduced a new technology potential to enhance the performance, functionality and device packaging density and to reduce the power consumption and cost having multiple active layers stacked. The increase in current demand and faster switching frequency of the stacking, introduce critical power integrity and reliability challenges compared to conventional system on chip. As a result stacked dies with dense through silicon vias requires a comprehensive modeling and analysis study.

Previous works [1], [2] addressed power integrity analysis of the 3D power distribution networks (PDN). *Huang* et al. [1] established an analytical 3D PDN model considering the TSV and package effective inductance One of the major applications of the 3D ICs is heterogeneous integration of multiple power levels such as digital and DSP cores, memory, RF and analog modules that are stacked together [3]. Substrate coupling modeling is a key issue due to its significant impact on the performance of the analog circuits on the stacked chip. In this work, a comprehensive frequency dependent model for through silicon via and power grid of stacking layers with substrate coupling among the TSVs is presented.

*Shayan* et al. in [4], presented a reliability aware TSV planning considering thermo-mechanical stress. We adopt the methodology in [4] and proposed model for the substrate coupling and analyzed the impact of frequency dependent TSV and substrate parasitics on the voltage variation. The reliability model is extended to include the electromigration constrains. The benefit of saving block out space in favor of decoupling capacitor placement is presented. The paper proposes a unified methodology to address the problem of optimally design of the 3D stacking under reliability constraints i.e., one with the following properties and constraints: (i) minimum IR drop across the power grid in layers and including substrate coupling among the TSVs and tiers, (ii) satisfy electro migration maximum current density constraints (iii) maximizing lifetime and thermo-mechanical reliability of the chip and finally (iv) maximizing area for routability and decoupling capacitors allocation. Eletromigration (EM) [5] and thermo-mechanical [6] stress is the root cause of major long term failure problems in 3D stacked ICs which is the focus of this work.

First, the TSV and stacked grid electrical modeling scheme is presented considering the substrate coupling. The benefit of frequency domain is that we can incorporate the frequency dependent parasitic as well as we could high light the resonant peak. The extracted model demonstrates variation in frequency domain which could not be ignored as oppose to fixed parasitic model. The time domain transient response is recovered using vector fitting [2]. The stacked grid is analyzed for power noise and reliability. The 3D design is formulated as an optimization formulation to obtain minimum noise under reliability constraints.

The remainder of this paper is organized as follows: In section II, the details of 3D power distribution model is presented. Substrate coupling model among the TSVs and tiers are extracted as a frequency dependent electrical model section III discusses, frequency domain based flow which is used in this work for power integrity analysis of 3D PDN model. In section IV, details regarding the electro migration and thermo mechanical reliability aspects are discussed. Section V, presents our formulation for the design of a reliable stacked IC power distribution and experimental results and finally section VI concludes the paper.

## II. 3D PDN model with substrate coupling

In this section, analytical fitted model and extractions of the through silicon via and power grid in each tier is presented considering presence of the silicon substrate coupling. One of the key technologies that enable stacking multiple dies in system in package (SiP) is through silicon via. Heterogeneous dies with different functionalities and high operation frequency are stacked densely. The silicon substrate is usually of low resistivity in digital ICs and this will lead to silicon substrate propagation during power delivery and as a result noise.

978-1-4244-5028-2/09/$25.00 ©2009 IEEE

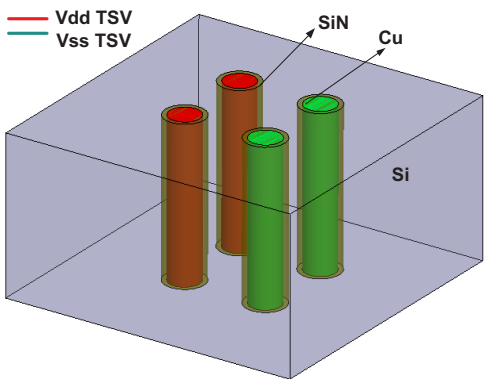


Fig. 1. Through silicon via model in HFSS

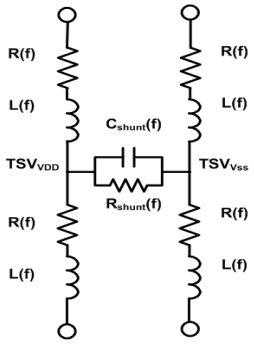


Fig. 2. TSV RLGC equivalent $RLCG(f)$ model with substrate coupling

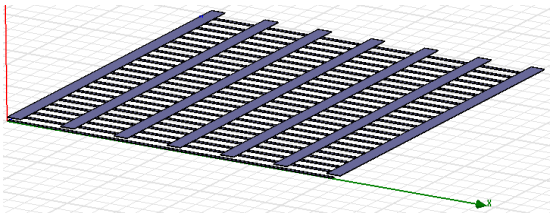

Fig. 3. Power grid model in each layer

To the best of the authors knowledge, none of the previous work on 3D power distribution [4], [1], [7], modeled and considered the impact of substrate coupling in power noise. One challenge that is introduced as a result of three dimensional stacking is parasitic interactions through the shared silicon substrate and among TSVs. Each time transition and switching occurs in the digital circuits, switching currents working in conjunction with circuit and through silicon via parasitic, inject noise into three dimensional stacked packages. The silicon substrate is conductive and power noise easily propagates to analogue circuits destructively impact their performance due to deficient immunity of digital circuits [8]. In next section, the through silicon via model and extractions are described.

### A. Through Silicon Via Model

The structure of Through Silicon Via (TSV) is shown in Figure 1. At higher frequencies current does not flow uniformly across the cross section of the conductor. Instead the current becomes increasingly concentrated near the edge of surface which is called skin effect and current densities vary with respect to frequency. As a result, the effective cross section area is reduced with the onset of skin effect, causing the effective resistance at high frequencies to increase. Previous work [9][10] addressed modeling the TSV for single frequency and without consideration of the substrate coupling and tier to tier coupling effect. The proposed modeling take into account the frequency dependent parasites and substrate coupling and tier to tier grid effect to reflect more realistic and accurate TSV parasitic. The TSV is electrically modeled and extracted using High Frequency Structure Simulation (HFSS) full wave solver from Ansoft [11] to consider the substrate loss of TSV.

For the TSV structure modeling, the following properties are assumed:

1) The TSV is modeled as an array pair sets of $V_{DD}$ and $V_{SS}$ in the $200 \times 200$ $\mu m^2$ geometry having a silicon shared substrate through wafer via hole with insulation barrier formed on the substrate and via sidewall.
2) The substrate is a low resistive ($10\ \Omega \cdot cm$) silicon with small loss tangent ($< 0.0005$) [12]. The substrate loss could be mitigated by using high resistivity or thick dielectric as an expensive packaging alternative solution [13] based on application demand.
3) The TSV height is 100 $\mu m$.
4) The thin dielectric layer (silicon nitride) surrounding the TSVs is 0.2 $\mu m$ thick with $\varepsilon_r = 7$.
5) The model is extracted over broad frequency range of $50MHz$ to $10GHz$.

The dimensions of the through silicon via and the density of the TSV pitch varied and explored in the extractions in order to reduce the power noise to maximize reliability. The S-parameters of the $V_{DD}$ and $V_{SS}$ pairs are obtained from the extraction. The S-parameter of the TSV is converted to equivalent RLGC electrical model as described in section II-B.

### B. Substrate Coupling Model

The extracted S-parameters model for TSV is converted to equivalent fitted electrical model (Figure 2) following [14] where $\gamma$ is the propagation constant and Z is the TSV transmission line based characteristic impedance:

$$\gamma = \sqrt{(R + j\omega L) \cdot (G + j\omega C)} = \alpha + j\beta \tag{1}$$

$$Z = \sqrt{\frac{(R + j\omega L)}{(G + j\omega C)}} \tag{2}$$

From $Z$ and $\gamma$, equivalent fitted electrical $RLGC$ model is derived as follows which could be incorporated into frequency domain analysis flow:

$$R(f) = Re\{\gamma \cdot Z\} \tag{3}$$

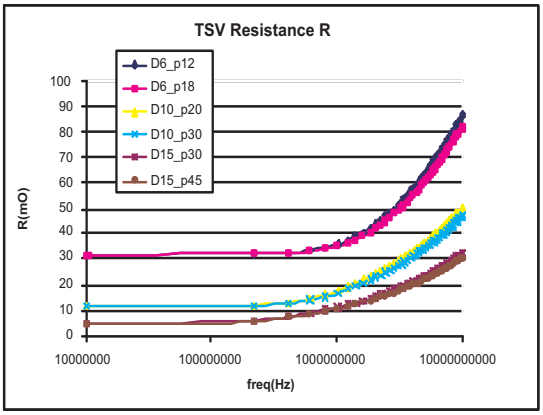


Fig. 4. TSV equivalent resistance R (D=diameter, P=pitch)

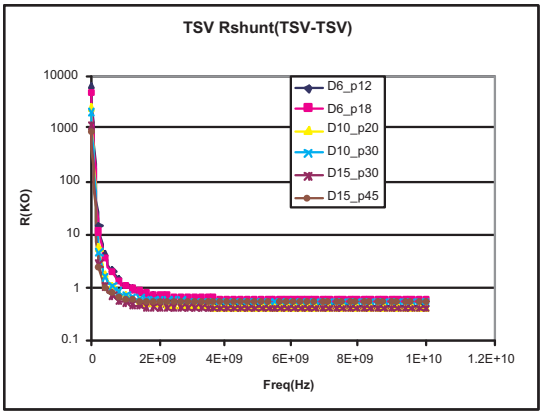


Fig. 6. Substrate equivalent shunt resistance (D=diameter, P=pitch)

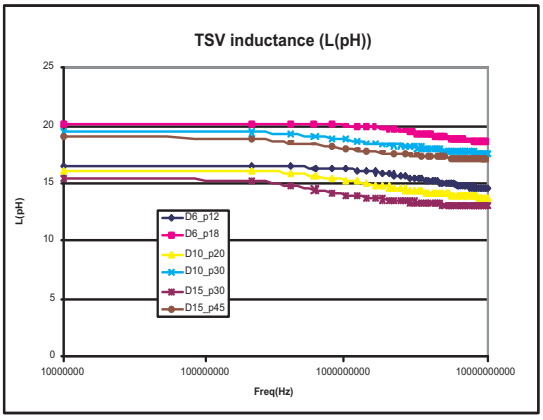


Fig. 5. TSV equivalent inductance L (D=diameter, P=pitch)

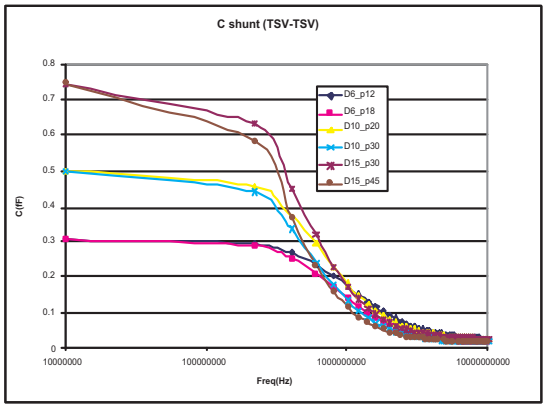


Fig. 7. Susbtrate equivalent shunt coupling (D=diameter, P=pitch)

$$L(f) = Im\{\gamma \cdot Z\}/\omega \tag{4}$$

$$R_{substrate}(f) = R_{shunt}(f) = Re\{\gamma/Z\}^{-1} \tag{5}$$

$$C_{substrate}(f) = C_{shunt}(f) = Im\{\gamma/Z\}/\omega \tag{6}$$

Figure 4 to Figure 7 are complete set of TSV extraction for different combination of TSV dimension and density. The TSV parasitic are then concatenated to represent the total stacked die (in the test case $1 \times 1$ $mm^2$) based on the $200 \times 200$ $\mu m^2$ sections.

### C. Power Grid Model in Each Tier

The power grid parasitic in each layer of stacked PDN is extracted for a $200 \times 200$ $\mu m^2$ geometry and concatenated as a lattice grid electrical model. Q3D Extractor [15] is used to extract the frequency dependent parasitic of each layer grid (Fig. 3). Two tiers are stacked together with TSV in the extractions in order to model the stacked grid.

Figure 5 illustrates that inductance depends on the pitch and diameter aspect ratio (pitch/diameter). The resistivity due to skin effect is a function of the TSV diameter as shown in Fig. 4 to Fig. 7 depicts that in high frequency (over $1GHz$) substrate coupling decreases significantly.

## III. 3D PDN ANALYSIS METHODOLOGY

For this section, we will describe the flow we developed for the analysis of the TSV and 3D power networks to identify the resonance peak as well as the maximum voltage drops. Most of the conventional simulator fails to simulate the system in a reasonable time because of the large scale number of grid in the 3D PDN. Figure 8 depicts our own developed package which is an efficient parallel processing analysis flow for the full power distribution network in both frequency and time domain.

In order to convert the frequency domain results into time domain we use vector fitting. The clock frequency of the 3D stacked ICs is reaching $GHz$ range where the SSN from the $di/dt$ cannot be ignored. In each frequency point, the frequency dependent $RLGC(f)$ is inserted into linear solver and the time domain is recovered using vector fitting. Conventional vector fitting [16] has unacceptable error range

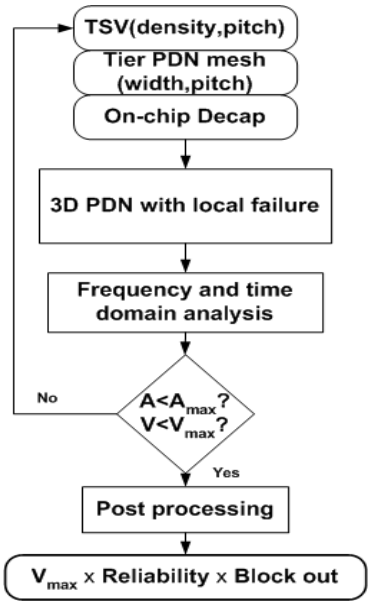


Fig. 8. 3D PDN reliability analysis flow

and the time domain recovered result has a large error ($\Delta VF$):

$$\Delta V_{VF} = V(t) - V_{VF}(t) \tag{7}$$

Here $\Delta VF$ is the deviation of the fitted time domain approximation and the original signal. We enhanced the vector fitting process and use the remainder of the vector fitting $\Delta VF$ and perform the vector fitting process iteratively until $\Delta VF$ reaches the acceptable error margin rate of $10^{-16}$.

## IV. Reliability of stacked power grid

The reliability of a system is defined as the probability function $R(t)$, over the interval $[0,\infty]$ that the system operates without any failure. The reliability is defined as function of failure rate, $\lambda_f(t)$ or alternatively with Mean Time To Failure ($MTTF$) where $MTTF = 1/\lambda_f$ . In our analysis, we use constant failure rate reliability. The component reliability could be represented by using exponential distribution [17] with a failure rate $\lambda_f$ as (8):

$$R(t) = e^{-\lambda_f(t)} \tag{8}$$

### A. Electromigration Constraint

For each power grid node i: $\Delta V_i(t) \leq \Delta V_{max}$ where $\Delta V_{max}$ is about 5% of nominal $V_{DD}$ for nanoscale technology according to delay corners. Electromigration (EM) is major cause of momentum transfer from electrons to the ions which make interconnect lattice. In 3D IC, electromigration due to higher current variation and density, will lead to shortening between adjacent metal layers, TSV and bumps; opening of metal lines and TSV contacts and increased resistance of metal lines and TSV contacts. The mean time to failure (MTTF) due the EM is described by the Black's model as in [18]:

$$MTTF_{TSVEM} = k_{bondingTSV} A_\circ (J - J_{crit})^{-n} \frac{E_a}{kT} \tag{9}$$

Here, $A_\circ$ is an empirically determined constant, $J$ is the current density in the interconnect, $J_{crit}$ is the threshold current density and $K$ is the Boltzmann's constant, $E_a$ is the activation energy and $n$ is scaling factor (usually set to 2). EM in stacked wire segment sets an upper bound on the average current density, thus impose a minimum wire width constrain. For a fixed thickness $t_k$ of a layer $k$ and the given maximal current density $J_{crit}$, this constraint for a wire segment between node $i$ and $j$ can be expressed as:

$$|\frac{1}{T}\int_0^T (V_i(t) - V_j(t))\,dx| \leq J_{crit} \cdot \rho l t \tag{10}$$

Where $\rho$ is the sheet resistance, $l$ is the length of the wire segment, $V_i(t)$ is the voltage at node $i$, and $V_j(t)$ is the voltage at node $j$ and $T$ is the period. Therefore the EM rule imposes either a minimum width of the wire with given power bus pitch or a minimum pitch with given wire width.

Black model that is used here for EM constraint is extended to take into account TSV exclusive EM factor due to the bonding. Stacked TSVs would have a bonded interface that may be Cu-Cu, or Cu-tin alloy bond. In additional to material differences, bond quality would also affect EM. $k_{bondingTSV}$ bonding coefficient in 9 is the TSV empirical bonding coefficient and is provided by the fabrication company.

### B. Stacked Die Thermo-mechanical Reliability

Stacked ICs, thermo-mechanical modelling and analysis are crucial step in the design of a reliable 3D PDN. Global thermal mismatch between the copper filled TSV substrate and silicon chip is large and the micro bumps would break under thermal conditions. Global thermal mismatch depends on both the TSV size and pitch. The coefficient of thermal expansion (CTE) of copper ($\sim 17.5\mu/^\circ C$) is much higher of the silicon CTE ($\sim 2.5\mu/^\circ C$) [6]. Due to thermal cycling and local thermal expansion mismatch between the copper and silicon substrate the stacked die has the delimitation potential in the interface of the TSV, dielectric, substrate, and grid [19]. $\lambda_{TM}$ , effective stress and thermo-mechanical failure rate of the TSV increases as either the TSV diameter reduces or density reduction [6]. *Selvanayagam* et al. [6], performed a comprehensive study on thermo-mechanical stress and strain for multiple TSV dimensions. The thermal stress will degrade if the density of the TSV increases due to reduction in thermal resistance. Figure 9 depicts the normalized thermo-mechanical failure for various TSV densities and dimensions. TSV density(%) in Figure 9 is the TSV pitch percentage from maximum allocable TSV nodes.

## V. Experiments and analysis

The proposed problem formulation is described in this section to derive the optimal reliable design parameters, i.e. TSV diameter and pitch for the stacked power distribution. The main objective of the optimization is to minimize the power noise while maximize the reliability. In the design of the 3D PDN, two main constraints needs to be satisfied:

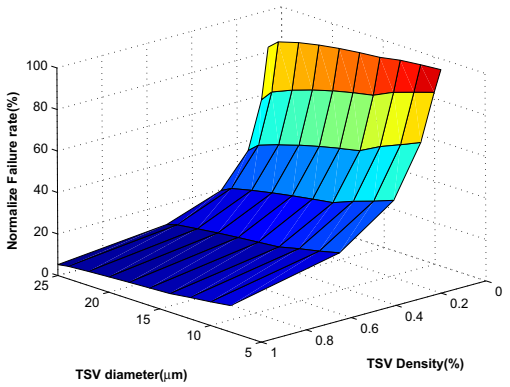


Fig. 9. Normalized TSV thermo-mechanical failure rate(%)

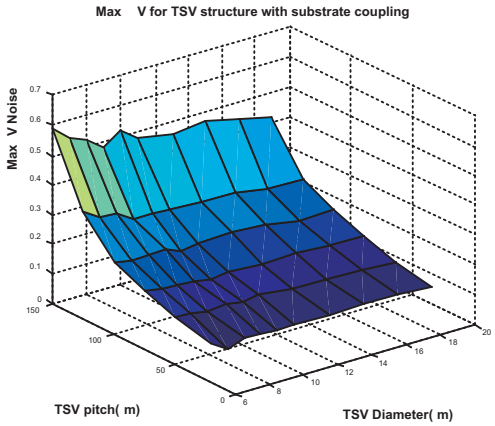


Fig. 11. 3D stacked power noise (volt) with substrate coupling model.

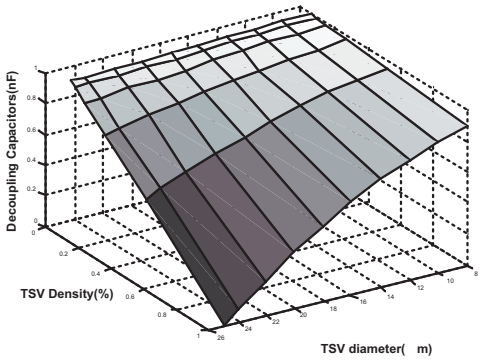


Fig. 10. Decoupling capacitor allocation trade off vs. TSV allocation.

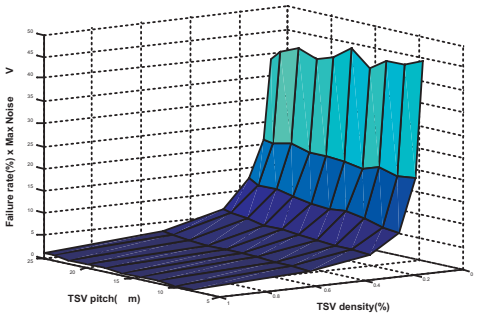


Fig. 12. Optimization cost function($Failurerate_{TSV} \times max\Delta V$).

1) *Electromigration current density*: Current density should be less than the Electromigration maximum current density as described in section 4.1.
2) *Maximum routable area*: According to DRC rules, surrounding TSV there is a block out region where no hard macro could be placed. The blocked area should be limited by the maximum area dedicated to hard macro placement.

In addition, we define decoupling capacitor allocable area as $A_{decap} = k_{decap} \times A_{routable}$ where $k_{decap}$ is percentage of the routable area ($A_{routable}$). Therefore; there is a trade off between having dense TSVs with large dimensions versus allocating more decoupling capacitors among tiers in the unblocked area (Figure 10).

The optimization problem is formulated as:

$$Min : Failure \times (\Sigma_i \Delta V_{maxTSV} + \Sigma_j \Delta V_{maxtier}) \qquad (11)$$

*s.t.*

(I) $A_{blockout} \leq min(A_{routable})$

(II) $|\frac{1}{T}\int_0^T (V_i(t) - V_j(t))\,dx| \leq J_{crit} \cdot \rho l_{p,q} t_{\ p,q}\, \varepsilon\ 3DPDN$

$$Failure(TSV_{diameter}, TSV_{density}) = 1 - R(t)$$

The objective is to minimize total power noise in TSV which are $\Delta V_{iTSV}$ and in stacked layers $\Delta V_{jtier}$. The keep out area in constraint $(I)$ should be less than minimum routable Area. $(II)$ satisfies the EM maximum current densities (IV-A). $R(t)$ is the reliability function as described in section IV.

### A. Reliability analysis

In the experiments, we model $1 \times 1\ mm^2$ 5 layers stacked dies with the tier-to-tier height of 100 $\mu m$. Different diameters of the through silicon via is modeled and extracted. The current sources in each layer represent the active die switching profile. The amplitude of the current triangular sources is maximum power divided by the supply voltage and number of the nodes. Based on our flow described in section III, the maximum power noise is obtained (Figure 11). We approximate the maximum voltage noise and reliability with a polynomial expression function TSV diameter and pitch to solve the TSV linear optimization.

Figure 12 demonstrate the impact of number of stacking layer on power noise. Finally Figure 12 illustrates proposed

cost function from optimization scheme where the optimum configuration is derived. Figure 12 depicts that based on the TSV density and diameter the optimal point is where the TSV density is the highest and the TSV diameter is in the middle to minimize noise and maximize reliability. The noise value and reliability value is fitted into a polynomial expressions to derive the optimal cost function.

## VI. Conclusions

In this paper, a comprehensive 3D PDN stacked model is introduced. The model specifically addressed the substrate coupling of the 3D power grid and TSV with frequency dependent parasitic. The S-parameter model is converted into $RLGC(f)$ electrical model so that we can incorporate it into the frequency domain analysis flow. Electromigration current density constraint and reliability issues were focused on this work . An optimization problem formulation is introduced with objective of minimizing power noise under reliability constraints. The experimental results demonstrate efficacy of the proposed framework.

## References


[1] G. Huang, M. Bakir, A. Naeemi, H. Chen, and J. D. Meindl, "Power delivery for 3d chip stacks: Physical modeling and design implication," in *IEEE Electrical Performance of Electronic Packaging, 2007*, Oct. 2007, pp. 205–208.

[2] A. Shayan, X. Hu, H. Peng, M. Popovich, W. Zhang, C. Cheng, L. Chua-Eoan, and X. Chen, "3d power distribution network co-design for nanoscale stacked silicon ics," *Electrical Performance of Electronic Packaging*, 2008.

[3] S. Lim, "Physical design for 3d system on package," *IEEE Trans. Design and Test of Computers*, vol. 22, no. 6, 2005.

[4] A. Shayan, X. Hu, H. Peng, C. Cheng, W. Yu, M. Popovich, X. Chen, and T. Toms, "Reliability aware through silicon via planning for nanoscale stacked silicon ics," *Design Automation and Test in Europe*, 2009.

[5] R. Labie, W. Ruythooren, K. Baert, E. beyne, and B. Swinnen, "Resistance to electromigration of purely intermetallic micro-bump interconnections for 3d-device stacking," *Interconnect Technology Conference*, 2008.

[6] C. Selvanayagam, J. H. Lau, X. Zhang, S. K. W. Seah, V. Kripesh, and T. C. Chai, "Nonlinear Thermal Stress/Strain Analyses of Copper Filled TSV (Through Silicon Via) and Their Flip-Chip Microbumps," in *Electronics Components and Technology Conference, 2008*, May 2008, pp. 1073–1081.

[7] J. Sun, J.-Q. Lu, D. Giuliano, T. P. Chow, and R. J. Gutmann, "3D Power Delivery for Microprocessors and High-Performance ASICs," in *IEEE 22nd Applied Power Electronics Conference, 2007*, Mar. 2007, pp. 127–133.

[8] M. Heijningen, M. Badaroglu, S. Donnay, G. Gielen, and H. D. Man, "Substrate noise generation in complex digital systems: efficient modeling and simulation methodology and experimental verification," *IEEE Journal of Solid-State Circuits*, 2002.

[9] A. Rahman, J. Trezza, B. New, and S. Trimberger, "Die stacking technology for terabit chip-to-chip communications," *Custom Integrated Circuits Conference*, 2006.

[10] S. Alam, R. Jones, S. Rauf, and Chatterjee, "Inter-strata connection characteristics and signal transmission in three-dimensional (3d) integration technology," *International Symposium on Quality Electronic Design*, 2007.

[11] "http://www.ansoft.com/hfss/."

[12] S. Ho, S. Yoon, Q. Zhou, K. Pasad, V. Kripesh, and J. Lau, "High rf performance tsv silicon carrier for high frequency application," *Electronic Components and Technology Conference*, 2008.

[13] R. Yang, C. Hung, Y. Su, M. Weng, and H. Wu, "Loss characteristics of silicon substrate with different resistivities," *Microwave and Optical Tech. Lett.*, 2006.

[14] W. Eisenstadt and Y. Eo, "S-parameter-based interconnect transmission line characterization," *IEEE trans. on Components, Hybrids, and Manufacturing Technology*, vol. 15, no. 4, 1992.

[15] "http://www.ansoft.com/products/si/q3d_extractor."

[16] W. Zhang, L. Zhang, R. Shi, H. Peng, Z. Zhu, L. Chua-Eoan, R. Murgai, T. Shibuya, N. Ito, and C. K. Cheng, "Fast Power Network Analysis with Multiple Clock Domains," in *25th International Conference on Computer Design, 2007*, Oct. 2007, pp. 456–463.

[17] B. Epstein and I. Weissman, "Mathematical models for systems reiability," *Mathematical Models for Systems Reiability*, 2008.

[18] T. Rosing, K. Mihic, and G. D. Micheli, "ower and reliability management of socs," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, 2007.

[19] P. Arunasalam, F. Zhou, H. Ackler, and B. Sammakia, "Thermo-mechanical analysis of thru-silicon-via based high density compliant interconnect," *Electronic Components and Technology Conference*, 2007.