Defect-Based Test Optimization for Analog/RF Circuits for Near-Zero DPPM Applications

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***Abstract*— Analog circuits are often tested based on their specifications. While specification-based testing ensures the initial product quality, full testing is often not possible in high volume production. Moreover, even full specification-based testing cannot guarantee that the circuit does not contain any physical defects. Some application domains require near-zero defect levels independent of whether the specifications are met. In this work, we present a defect based test optimization method focusing on defective parts per million (DPPM) minimization. We extract potential defects through inductive fault analysis (IFA) and reduce the number of tests without degrading the test quality. In order to achieve near zero DPPM, we employ outlier analysis to identify defective circuits that cannot be identified using specification based methods. Simulation results on an LNA show that DPPM is reduced down to 0 at a cost of 0.2% yield loss with the proposed method.**

I. Introduction

The objective of test optimization methods have been to shrink the test list or reduce the test cost using alternative test methods [1], [2]. Some application areas, however, require near-zero level defective parts. Such a low defect level cannot be guaranteed even if full specification tests are conducted. There may be devices that satisfy all the specifications but still have defects, which affect their reliability. It has been reported that defects are the primary cause of customer returns [3]. For application areas that cannot afford reliability risk or the cost of return, it is imperative to detect all defective devices.

Difficulty in identifying the defective devices rises from the fact that some defects alter the circuit behavior only slightly and process variations may mask their manifestation on the specifications. Defect oriented test methodologies [4], [5] have been proposed to address the requirement of low-cost defect screening. Defect-based test generation and optimization enables even small test lists to identify a large portion of the defects. Defect-oriented testing is performed in three steps: defect list generation, defect simulation, and screening.

Physical defects have typically been modeled with extremely simplistic circuit behavior [6], [7], [8] , namely as open and short catastrophic defects having a fixed resistance value typically on the order of $1M\Omega$ and 1Ω respectively [7]. Presently, more sophisticated models of various defects have been proposed in [9], where S-parameters of defects are extracted using an electromagnetic simulator. These realistic models help capturing the true behavior of the defects.

If the defect list generated at circuit level, it is probable to obtain defect list of size ranging from hundreds to thousands. However, in practice only a small subset of these defects are likely to occur. Inductive fault analysis (IFA) method has been proposed [10] to generate a realistic list of defects using layout level information. IFA has been shown to significantly reduce the number of defects for a given circuit [8].

For applications that require near-zero defect-levels, alternative identification methods are needed. One option is to tighten the specification limits so as to prune away devices with slight shifts from the nominal. However, this approach would incur significant yield loss for the near-zero defect-level. Additional specification tests or alternative test strategies have been proposed to increase the degree of freedom in order to detect defective devices without degrading the yield. Iddq test [11], [12] is a commonly used low-cost technique. However, it is not capable of identifying all defects. Indirect test methods are used to reduce test cost by employing test set-ups for easy to measure parameters and mapping these results are mapped back to the performance domain [2]. Outlier based methods are also used to improve defect coverage [3]. Machine learning methods have been shown to be effective in defective device identification [13], which can also be used on defect identification.

All the abovementioned approaches require generation and analysis of alternative test stimuli that would eventually exercise and distinguish defective behavior. However, there is no systematic way of determining the best test stimuli. A novel test stimulus also requires design and validation of new test set-ups and would place a high overhead on the test development process. Moreover, none of the previously proposed techniques have been shown to reduce DPPM to near-zero levels. In this work, we aim at reducing the number of tests and achieving 100% defect identification level, while keeping yield loss at an acceptable level. We still rely on the original specification measurements, thus require no additional test set-up. We employ two-dimensional outlier analysis in order to identify even minute perturbation of behavior. Our technique requires a very small computational overhead, placing virtually no additional time on the critical path.

Our motivation behind selecting specification-pair outlier analysis is its simplicity of integrating into the production line and its ability of identifying abnormalities in performance. Although defects cannot be identified using

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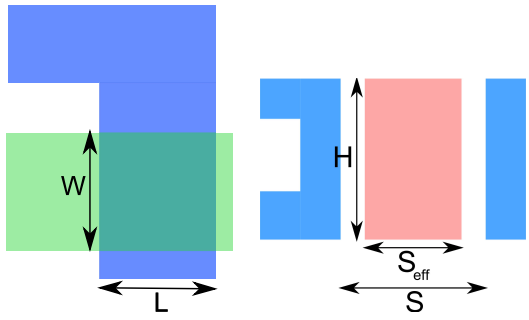


(a) (b)

Fig. 1. Overlap and Separation type defects

specification tests alone, outlier analysis greatly increases the chance of identification. Our method is composed of two parts. During off-line analysis, a minimal set of outlier specification-pairs are obtained, where only outlier pairs that contribute to defect identification are selected. During the actual test phase, this minimal set of outlier pairs are used, hence computational burden is greatly reduced. Outlier-pair-list generation is done with the objective to minimize the number of tests. Experimental results show that 40% of test size reduction from the full specification list is achieved with zero DPPM level.

II. Defect Based Testing

Accuracy and relevance of a defect list depends on how much information about the device is used in defect extraction. Using lower level information gives more detailed information about the device. Inductive fault analysis (IFA) method uses layout level information to obtain the possible defects given the defect scenarios.

Systematic or large scale defects are easy to detect and can be usually detected using simple tests. However, random spot defects are hard to detect, since the disturbance they cause may be insignificant to observe. In this work, we focus on random spot defects. The reasons of spot defects can be summarized as dust particles, extra or missing material, missing or broken contacts and broken wires. Using the IFA method we conduct layout level analysis to identify possible defect locations.

In order to locate possible defects, we need to know size and layer at which defects reside. There are two methods [14], [15] in defect simulation; we employ critical area based approach [15]. We determine critical areas on the layout where defects are possible to cause a damage on the device and calculate the probability of occurrence of the defect. One of the defect scenarios is electrical connection between two different layers, such as pinholes and extra vias, resulting in overlap type defects. Figure 1(a) shows a typical scenario of an overlap type defect, where the shaded area indicates the critical region for the overlap defect. Probability of occurrence of this defect can be calculated using eq (1):

$$\#\text{ of defect}_i = W \times L \times Density(defect_i) \quad (1)$$

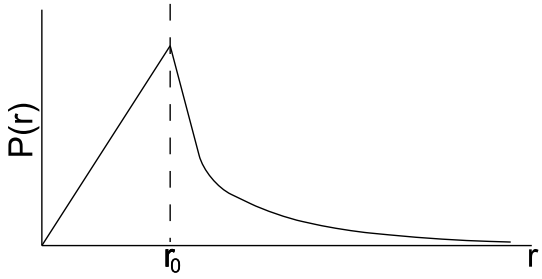


Fig. 2. Defect Size Distribution

where L, W and Density($defect_i$) are length, width and defect density of i^{th} defect respectively. Another type of likely defect is the bridge defect which is defined as a short between metals of the same layer. A bridging defect is illustrated in Figure 1(b). This type of defect is due to an extra layer of metal shorting two separate wires. In order to calculate defect occurrence probability of this defect we need size information of the defect. Various defect size distributions have been proposed [6]. We use the defect distribution model presented in [14], as shown in Figure 2, while the probability distribution curve given in [14], [6]. r_0 is a parameter of the curve; it is usually taken as the minimum feature length of the process. $Density(defect_i)$ is the density of i^{th} defect and is process dependent. Defect occurrence probability of this defect type is calculated using eq (2-3):

$$\#\text{ of defects } = W_{eff} \times L \times Density(defect_i) \quad (2)$$

$$W_{eff} = 2\int_{W/2}^{W}\int_{0}^{r} defectSize(\alpha)\, d\alpha\, dr \quad (3)$$

Another type of hard defects is open circuit defect. Examples for open type defects are cracked wires, missing vias and missing materials. Probability calculation of these defects can be conducted in a similar manner to the probability calculation of short circuit defects based on critical areas and defect densities.

Given the critical areas of the defects and defect densities, we can easily calculate defect occurrence probabilities. However, we may not have the absolute defect density information for a particular technology. Fortunately, relative defect density information can also be used to calculate defect probabilities. A typical relative defect density information is tabulated in Table I. First five values of the table are based on published data [16], while last two are assumed due to lack of published data. Substituting relative density values in open defect and short defect calculation equations, we can compute relative defect probabilities. Equation 4 can be used to calculate relative defect probability of each defect, where the denominator is the normalizing term.

$$P(defect_i) = \frac{W_i \times L_i \times Density(defect_i)}{\sum_i W_i \times L_i \times Density(defect_i)} \quad (4)$$

Layer	defect	relative density
Metal1	open	0.01
Metal1	short	1
Metal2	open	0.02
Metal2	short	1.5
via	open	0.8
M1-M2	pinhole	1
M1-P1	pinhole	1

TABLE I
RELATIVE DEFECT DENSITY

A. Defect Model

Possible defects that are identified using the IFA method are injected into circuit-level representation to perform defect simulations.

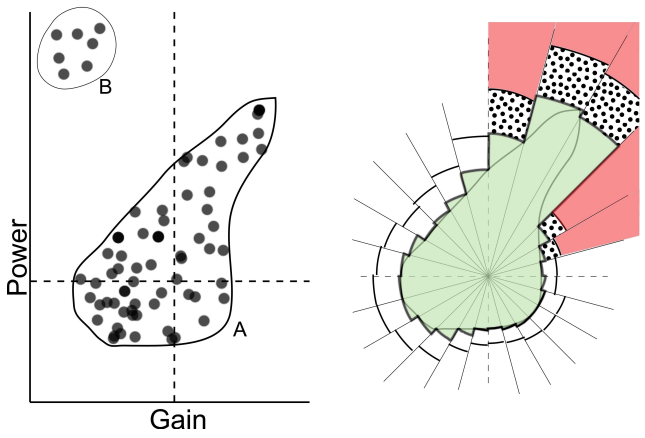
Defect models used in literature are usually small resistances for shorts and very large resistances for open circuits [7], [8], [6]. Although simple, most of the time these models may not provide the desired accuracy to observe the true behavior of the defects. Acar *et. al.* conducted electromagnetic simulations for various types of defect scenarios and obtained frequency dependent response of the defects [9]. We use these electrical models in our simulations.

III. TEST METHODOLOGY

Testing devices for their specifications identifies functionally acceptable (good) and unacceptable (bad) devices. However, a good device is not necessarily defect free. Therefore, it is important to take additional steps in addition to specification tests to find out the defective devices. In this work, we focus on outlier based testing method to identify the defective devices.

An outlier device is defined as a device that behaves substantially different compared to the bulk of devices. One way of conducting outlier analysis is to tighten the limits of the test measurements to below their specifications. However, due to high process variations, defect level can only be substantially reduced if the yield is sacrificed to a great length.

Luckily, we can take advantage of proximity-based correlations in process variations to overcome this problem. Even if process variations cause circuit parameters to widely vary, the relation between two measured parameters may be unaltered if they are structurally correlated. This is due to the fact that most process variations are caused by die-to-die fluctuations whereas within-die fluctuations are very small. This premise is widely used in analog circuit design where the ratios of matched components, rather than their absolute values, define the overall behavior. Defects alter the circuit structure, hence the correlation patterns of the specifications. Thus, defects can be detected by identifying devices outside of the expected correlation patterns. In this sense, the behavior of a circuit with respect to two specifications at once can be analyzed to take advantage of specification correlations. Outlier analysis can be conducted in this two dimensional space. As an example, suppose that two of the specifications of a circuit is *gain* and *power consumption*. If we plot the outcomes of measurement/simulation for gain with respect to power consumption, we can analyze the relation between two specifications. Figure 3 illustrates a typical gain-power consumption relation of a LNA in the presence of process variations. In this figure, region A shows the region where defect-free devices reside. Knowing the behavior of defect free devices on outlier diagrams, we can identify defective devices simply by checking wether devices are falling in the safe region. If a device falls out of the safe region, it is identified as a defective device. Region B shows the possibly defective devices since they behave substantially different than the majority of the device ensemble. Similarly, construction of outlier diagrams for various combinations of specifications reveals the hard-to-detect abnormalities and enables us to spot the defective devices.



(a) (b)

Fig. 3. Outlier Diagram

A. Outlier Analysis

Our defect identification method works in two phases; off-line phase and on-line phase. In the off-line phase, the analysis engine is trained with defect free devices to generate reference outlier diagrams. The first step does not contribute to test time since it runs prior to production testing. In the second phase, once the measurements are conducted, devices are identified with respect to expected correlation patterns.

In the off-line phase, correlation patterns are extracted, analyzed, and outliers are defined. As an example, suppose that we would like to store the outlier information for the gain-power consumption pair from Figure 3. The key point in representing this information is to model it in such a way that checking four outliers does not place a computational burden on the tester. For this purpose, we first shift the distribution so that it is zero-mean and then we normalize it with standard deviations of spec "A" and spec "B". Then, we convert the coordinate system to polar coordinates and divide the azimuth range into N bins as we illustrate in Figure 3(b). Now, we find the devices that have maximum distance from the origin in each bin and record these

```
Order Specs
for all (i, j) such that i ≠ j do
  Shift
  Normalize
  fails ← identify defectives
  if size(fails) ≥ 0 then
    append (i,j) → outlierPairs
    record LUT for (i,j)
  end if
end for
```

Fig. 4. Outlier Analysis and Test Selection Algorithm

distance values in a lookup table. Lookup tables generated for each specification pair draw a virtual boundary between defect free and potentially defective devices. However, this boundary may not be very accurate due to process variations and might result in misclassification of marginal devices. In order to avoid substantial yield loss, we insert a buffer between the defect free region and the defective region. We define the defective region relative to the defect free region using a ratio that we call *defect threshold ratio*. If the radius of the defect free region is r for a particular azimuth bin and the defect-threshold-ratio is $ratio$, then buffer region is in (r and $r \times ration$) range and defective region is in $(r \times ratio, \infty)$ range. The size of the buffer region controls the misclassification rate and defect coverage rate, a more thorough analysis is provided in the results section.

The on-line phase takes place during production testing. We utilize the lookup table generated in off-line phase for defect identification. The algorithm we use in on-line phase to eventually classify the devices as pass or fail is shown in Figure 5. For a given DUT, we go through the outlier specification-pair list. If the DUT falls into the defective region, it is immediately rejected. Otherwise, all specification pairs are exhausted before the DUT is accepted.

B. Test Development

Generation of lookup table for all possible specification pairs may result in excessive memory and CPU usage. If we have M specifications, exhaustive enumeration of all specification pairs will result in $M*(M-1)$ outlier diagrams. Measurement and computation for all these pairs is not affordable during production test. Moreover, specification pairs that do not display a structural correlation are of little use in identifying defective devices. Hence, we reduce the number of outlier-specification-pairs through selecting ones that contribute to defect coverage only. Figure 4 shows the algorithm we employ to determine the specification pairs for outlier analysis. Inputs for the algorithm are a defect free device set and a defective device set. Devices in the defective set have the same process variation but they are generated through injecting defects. We start with ordering the specification list by first placing the minimum covering specification test set at the beginning of the list [17]. The rest of the specifications are ordered according to the their potential of identifying defective devices. We use a metric

```
for all (i,j) in outlierPairs do
  Shift
  Normalize
  identify defectives
end for
```

Fig. 5. Pass/Fail Determination During Production Testing

that we show in eq (5) that is analogous to signal to noise ratio (SNR) in order to sort the specification list:

$$SNR_i = \frac{\mu_{ff,i} - \mu_{defective,i}}{\sqrt{\sigma^2_{ff,i} + \sigma^2_{defective,i}}} \tag{5}$$

where, $\mu_{ff,i}$ and $\mu_{defective,i}$ are mean values of defect free and defective devices respectively for i^{th} specification, while $\sigma_{ff,i}$ and $\sigma_{defective,i}$ are standard deviations. We iterate over the ordered list and evaluate the potential outlier pairs they form with the tests that have already been included in the test list. Defect identification rates are calculated for each potential pair using the number of incrementally identified devices. Lookup tables for specification pairs that result in nonzero defect identification are stored for later use in the on-line phase.

IV. Results

We evaluate of our method using a variable gain LNA, which is shown in Figure 6. The layout of this circuit, which we used to extract defect probabilities is shown in Figure 7. Possible defect types that are listed in Table I are extracted manually from the layout and defect probabilities are calculated for each defect type. Table IV shows significant defects, their type and relative probability of their occurrence. We omitted the defects that have low relative probability, since they do not contribute to DPPM. Hence, using the IFA approach, compared to all possible defects that can occur, we have only 15 potential defects that can occur for this LNA. Moreover, relative probability information provided in the table enables us to estimate the effect of each defect on DPPM. First 11 defects are node-to-node bridging defects, while defects 12 and 13 are open via defects. Defect 14 and 15 that are denoted with L_D and L_S respectively are short defects that reside in the inductors.

In order to find the detectability of the defects, 5k simulations are performed for each defect. Defect models from [9] are used for defect simulations, as has been mentioned in Section II. The process variation profile that we inject on the circuit is summarized in Table II. In addition to defect simulations, defect free device simulation of 40k samples were also performed. We also apply our method on defect free devices to find the yield loss of the method. 5k samples out of 40k defect free samples are used as training set, and the method is applied on the remaining 35k defect free samples.

If only specification based tests are used, 12 out of 15 defects can be identified. Therefore, assuming the yield level is 90%, a DPPM level of 4000 can be achieved, even

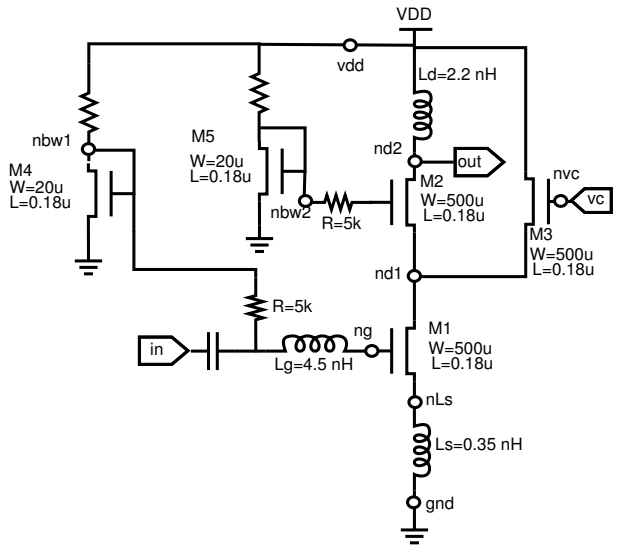


Fig. 6. LNA Schematic

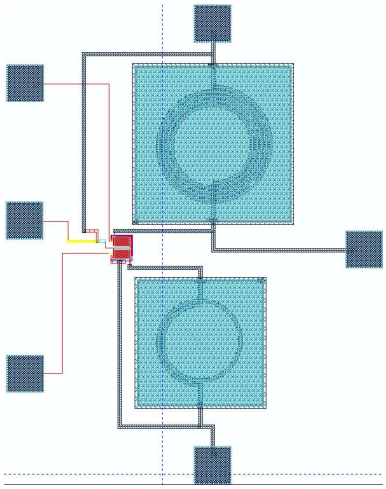


Fig. 7. LNA Layout

though we apply all specification tests. Specification based detectability is shown in table III. The goal of our method is to achieve near-zero DPPM, so the objective of applying this method is to reduce the DPPM level from 4000 to 0 for this particular case. For the off-line phase of our method, we use 5k defect-free devices to generate outlier-specification-pairs and LUTs for each of them.

Performance of our method is a function of two parameters that we have defined in section III; the number of bins in outlier diagrams and the defectiveness threshold level which determines the length of buffer region.

Table V shows defect identification performance of our method as a function of N and defectiveness threshold. Highlighted entries in the table constitute the feasible region in terms of defect coverage in order to achieve zero DPPM. Yield loss information is given in Table VI. N and defectiveness threshold levels that result in less than 1% yield loss are highlighted to show the potentially feasible region in terms of yield loss. Table VII shows the number of specifications that need to be measured for several N and defectiveness threshold pairs. These tables enable us to decide on the defect coverage versus yield loss trade-off. Since our premise is to achieve a DPPM level of zero, we need to select a combination of N and defectiveness threshold such that detectability is 100%.

Process variation	Width [%]	Length [%]	V_{TH0} [%]	Passive [%]
inter-die	0.1	2	2	2
die-die	0.3	5	5	5
lot-lot	1	15	15	13

TABLE II
PROCESS VARIATION

	L_d	L_s	nLs-gnd	others
detectability	89.08%	12.42%	91.28%	100%

TABLE III
SPECIFICATION BASED DETECTABILITY

Another criterion we need to consider is the yield loss, which should be as small as possible. Intersecting the highlighted regions of defect coverage and yield loss, we obtain a feasible region for both criteria. Among the feasible entries, the most relevant parameter combination is N=20 and threshold=1.2, which results in 0 DPPM and 0.2% yield loss. The number of specifications required to measure for this configuration is 31, as Table VII shows. Conducting the off-line phase, we have obtained the outlier-specification-pairs list and LUTs for each outlier diagram. The number of outlier pairs necessary for full detection is 80. Since we choose N=20 the total memory consumption of LUTs is 1600 8-bit entries.

For this circuit, 100% of defect coverage is achieved for all defects leading to zero-DPPM with resolution of 1 DPPM. One of the concerns in the online phase is the time required to do the computations. Based on simulations conducted using a 2.3GHz Quad core Intel machine, the time spent to identify each device is 1.5ms. Since total of 31 specifications are measured, computation time is 50μs per specification and since 50μs per is less than the time required for data acquisition, the computation overhead of the online-phase do not contribute to the overall test time.

Note that it is not possible to achieve 0 DPPM using specification tests even we conduct all tests. In our method however, only 31 specs are required to achieve 0 DPPM. Hence in terms of test size reduction, 40% of test list compaction is achieved.

V. CONCLUSION

Achieving near-zero DPPM during production testing is a requirement that needs to be met for application domains that cannot risk customer returns or involve mission critical operations. Most of the defective devices can be pruned away during production testing. However, some of them cannot be identified and treated equally as the defect free devices.

Defect	type	relative probability
nLs-gnd	M1-M1-short	0.0085
nd1-gnd	M1-M1-short	0.0124
nd1-nLs	M1-M1-short	0.3395
nd1-nd2	M1-M1-short	0.3350
nd1-nvc	M1-M1-short	0.0335
nd1-ng	M1-P1-pinhole	0.0532
nd1-nbw2	M1-M1-short	0.0003
nd2-gnd	M1-M2-pinhole	0.0131
nd2-nbw2	M1-P1-pinhole	0.0532
ndb1-gnd	M1-M1-short	0.0176
nbw2-vdd	M1-P1-pinhole	0.0185
R_{B1}	via-open	0.00023
R_{b1}	via-open	0.00023
Ld	M2-M2-short	0.0844
Ls	M2-M2-short	0.0303

TABLE IV

RELATIVE DEFECT PROBABILITIES

		Threshold					
		1.1	1.2	1.3	1.4	1.5	1.6
N	15	**100**	99.9994	99.9913	99.9736	99.8602	99.7552
	20	**100**	**100**	99.9922	99.9520	99.8464	99.7834
	40	**100**	**100**	**100**	99.9796	99.9982	99.7930
	60	**100**	**100**	**100**	99.9928	99.9598	99.9364
	80	**100**	**100**	**100**	99.9970	99.9922	99.9568

TABLE V

DEFECT COVERAGE [%]

		Threshold					
		1.1	1.2	1.3	1.4	1.5	1.6
N	15	**0.43**	**0.16**	**0.2**	**0.14**	**0.14**	**0.11**
	20	**0.66**	**0.2**	**0.15**	**0.09**	**0.12**	**0.67**
	40	1.5	**0.45**	**0.38**	**0.27**	**0.46**	**0.27**
	60	2.6	1.3	**0.67**	**0.76**	**0.68**	**0.79**
	80	3.87	1.79	1.53	1.16	1.13	**0.99**

TABLE VI

YIELD LOSS [%]

		Threshold					
		1.1	1.2	1.3	1.4	1.5	1.6
N	15	23	26	32	34	40	35
	20	29	31	37	35	37	38
	40	25	27	31	37	38	41
	60	29	28	34	37	38	40
	80	22	27	32	39	42	43

TABLE VII

OF SPECIFICATION THAT NEED TO BE MEASURED

Defects cause reliability problems and affect functionality of the devices. Hence, it is crucial to detect all defects. Defect identification problem has been previously addressed, however, none of the solutions were able to reduce DPPM to near-zero levels. In this work, we propose a defect-based low-cost test method that can attain near-zero DPPM levels employing a two dimensional outlier analysis method. We construct outlier diagrams of specification pairs and identify devices showing abnormal behavior. Two dimensional outlier analysis enables us to observe the perturbations caused by defects with a higher confidence, increasing the defect identification probability. We use only specification measurements in outlier analysis. Therefore, no additional test set-up or test stimuli generation is necessary. Moreover, computation burden we put on the ATE is very small.

We employ the IFA method to generate a realistic defect list and a relative occurrence probability table of the defects. The IFA method enable us to get a very compact defect set, while the probability table helps generate a realistic defect population for simulations. Simulation results show that for a particular LNA circuit, we are able to reduce the size of test list by 40% and DPPM level to zero at a cost of 0.2% of yield loss.

VI. ACKNOWLEDGMENTS

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