Hierarchical Parametric Test Metrics Estimation: A ΣΔ Converter BIST Case Study

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***Abstract*— In this paper we propose a method for evaluating test measurements for complex circuits that are difficult to simulate. The evaluation aims at estimating test metrics, such as parametric test escape and yield loss, with parts per million (ppm) accuracy. To achieve this, the method combines behavioral modeling, density estimation, and regression. The method is demonstrated for a previously proposed Built-In Self-Test (BIST) technique for ΣΔ Analog-to-Digital Converters (ADC) explaining in detail the derivation of a behavioral model that captures the main nonidealities in the circuit. The estimated test metrics are further analyzed in order to uncover trends in a large device sample that explain the source of erroneous test decisions.**

I. Introduction

Testing analog devices requires measuring the specified performances one by one and comparing them with their tolerance limits. This is the current practice because it is a head-on approach that guarantees the detection of out-of-specification devices while it accepts those that comply with the specifications. Any test escape or yield loss is due to measurement inaccuracies caused by, for example, tester calibration, software induced measurement instability and computation errors, contact issues in load boards and probe cards, multi-site tester differences, RF interference, etc. However, despite its high accuracy, specification-based testing incurs a very high cost.

Over the last two decades, several alternatives have been proposed towards reducing this cost. For example, structural testing relies on indirect tests that detect the presence of faults within the circuit [1], [2]. Other approaches include the compaction of specification-based tests [3], BIST [4], and alternate test techniques, wherein test measurements that are relatively easy to obtain are used to predict either the value of the specified performances through regression functions [5] or directly a Go/No-Go test decision through classifiers [6].

The aforementioned test alternatives provide a test decision that indicates the device quality, however there is hardly ever a proven equivalence between this test decision and the actual compliance or not to the specified performances. On one hand, there is a lack of widely acceptable analog fault models. On the other hand, it is highly unlikely that analog device performances would correlate perfectly with simple test measurements. To corroborate the claim that any test technique is equivalent to specification-based testing, it is needed to estimate the resulting parametric test escape and yield loss with a high level of precision, ideally at ppm levels. Moreover, this needs to be accomplished at the design stage so that design decisions that are required to facilitate low cost measurements will not need to be reconsidered at a later stage, in particular because re-spinning the design may not be possible at all due to cost and time-to-market constraints.

Recently, density estimation was considered for the estimation of parametric test metrics with ppm precision at the design stage [7]. However, this approach necessitates statistical Monte Carlo simulation at transistor level, which is too time consuming for complex circuits, such as signal converters and phase locked loops. In contrast, in this paper, we present a generally applicable approach to the problem of test metrics estimation. The idea will be demonstrated on a state-of-the-art BIST technique for ΣΔ ADC [8].

The remainder of the paper is organized as follows. In section II, we review previous work in statistical modeling of analog circuits. In, section III, we discuss the flow of the proposed method. Our case study is next described in section IV and results are presented in section V. Section VI concludes the paper with some directions for future work.

II. Statistical Modeling of Analog Circuits

Parametric test escape T_E and yield loss Y_L must be evaluated based on a set of devices that incur different combinations of design and process parameters (i.e. transistor geometry, flat band voltage, oxide thickness etc.). The design and process parameters are naturally sampled from their probability density function, thus resulting in an unbiased set of devices. Yet the size of the set needs to be very large in practice in order to obtain good estimates. To see this, consider a set of N devices. The Monte Carlo estimators of T_E and Y_L are given by

$$T_E^* = \frac{N_{C_g^c|T_p}}{N} \tag{1}$$

$$Y_L^* = \frac{N_{T_p^c|C_g}}{N} \tag{2}$$

where N_A is the count of the event A, C_g is the event that a circuit is good and T_p is the event that a circuit passes the test (the superscript c denotes the complementary event). For example, $C_g^c|T_p$ is the event that a circuit is faulty given that it passes the test. It can be shown that the variance of a Monte Carlo estimator T^* of a metric T is given by

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$$\sigma^2_{T^*} = \frac{T(1-T)}{N}, \tag{3}$$

which implies that an intractable number N of Monte Carlo circuit simulations is required to reduce the standard deviation σ_{T^*} to one order of magnitude less than T. For example, if $T = 10^{-3}$ (or 1000 ppm), then $N = 10^5$ in order to obtain $\sigma_{T^*} = 10^{-4}$ (or 100 ppm). A confidence level that T^* lies within ε of the true value T is given by Chebyshev's inequality

$$P\{|T^* - T| < \varepsilon\} \geq 1 - \frac{\sigma^2_{T^*}}{\varepsilon^2} \geq 1 - \frac{1}{4N\varepsilon^2}, \tag{4}$$

which shows that N must be quadrupled to achieve twice the accuracy. The foregoing discussion suggests that circuit simulation should be substituted by fast simulation of an approximative model of the circuit.

The problem of accelerating circuit simulation is met in various contexts, including design centering and sizing, design space exploration, verification, test stimuli optimization, fault simulation, test metrics estimation etc. Recent solutions find their roots in sensitivity analysis [9], density estimation [7], behavioral modeling [10], response surface modeling (e.g. regression) [11], and symbolic modeling with genetic programming [12].

Test metrics estimation with ppm accuracy is discussed in [7]. The idea is to extract the statistical law that gives rise to circuit simulation data. One disadvantage of this technique is that it requires to have access to initial simulation data from a number of circuits. This number increases exponentially with the number of test measurements and performances, in order to increase the approximation accuracy of the statistical law at its tails. In practice, good estimates can be obtained with a reasonable number of simulations, but still this number is prohibitive for complex circuits.

III. Hierarchical Parametric Test Metrics Estimation

Our approach to test metrics estimation for complex circuits is based on a combination of behavioral modeling, density estimation, and regression. Formally, let $A = [a_1, ..., a_{N_a}]$ be the vector of low-level design and process parameters and $X = [P,M] = [x_1, ..., x_{N_X}]$ be the vector of performances $P = [p_1, ..., p_{N_P}]$ and test measurements $M = [m_1, ..., m_{N_M}]$, $N_X = N_P + N_M$. The problem lies in developing a model F of the target circuit

$$X = [P,M] = F(A,I) \tag{5}$$

that can be easily simulated, where I denotes the stimuli required for obtaining X.

We first divide the circuit into blocks and, for each block, we develop behavioral models that capture the pertinent parameters which influence P and M, including the main non-idealities and non-linearities. Let $B = [b_1, ..., b_{N_B}]$ denote the vector of behavioral-level parameters. Still, it could be the case that the $N \gg 1$ behavioral simulations cannot be completed in reasonable time. In this scenario, another level of approximation needs to be added to accelerate behavioral simulation. For this purpose, N_X regression functions $g_j : B \mapsto x_j$, $j = 1, ..., N_X$, are learned that map B to X.

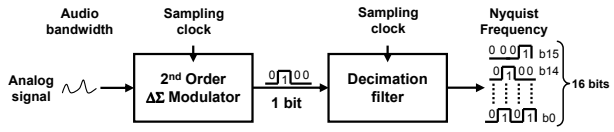

Fig. 1. Block diagram of a second-order ΣΔ ADC.

To perform a statistical analysis starting from A, it is necessary to model the mapping $g' : A \mapsto B$. One approach is to carry out standard circuit simulation following a divide and conquer approach, wherein the different blocks of the circuit are simulated separately (or in appropriate groups in case there are block-level parameters that are interdependent). However, this step can be very time consuming given the ultimate objective to simulate $N \gg 1$ circuit instances. For this purpose, we carry out only n simulations. The resulting n observations $B^0_{n \times N_B}$ of B serve for estimating the probability density function $f_B(B)$ of B. We follow the approach proposed in [7]. In particular, we use a nonparametric kernel density estimator which can approximate any underlying density even in the case where its marginals have distinct parametric forms. Subsequently, the density is sampled to generate a population $B^1_{N \times N_B}$ of $N \gg 1$ samples that is practically indistinguishable from the devices generated by a circuit simulator. In essence, this allows us to propagate the statistical distribution of A to B and perform the statistical analysis based on the intermediate behavioral-level parameters. The interested reader is referred to [7] for more details regarding the density estimation and sampling approaches.

The density $f_B(B)$ is also sampled n' times (typically $n' > n$) to generate a population $B^2_{n' \times N_B}$ that will be used in the training set for building the regression functions g_j. Unlike the sampling of $B^1_{N \times N_B}$ which is carried out with probability density function $f_B(B)$, the sampling of $B^2_{n' \times N_B}$ must be carried out such that it spans the feasible space of B. Next, n' behavioral simulations are carried out using $B^2_{n' \times N_B}$, which result accordingly in a population $X^2_{n' \times N_X}$ of vectors X. The training set $\left(B^2_{n' \times N_B}, X^2_{n' \times N_X}\right)$ is used to build the regression functions g_j.

Finally, the regression functions g_j are used to obtain the population $X^1_{N \times N_X}$: the j-th column of $X^1_{N \times N_X}$ is defined by $g_j\left(B^1_{N \times N_B}\right)$. Test metrics are calculated at ppm levels of accuracy based on the high-volume data in $X^1_{N \times N_X}$ using (1) and (2).

IV. Case Study: ΣΔ ADC

Oversampling ΣΔ ADCs have become very popular for high-resolution, medium-to-low speed applications. Oversampling dramatically relaxes the precision requirement for the analog circuitry at the expense of more complicated digital circuitry. This is very convenient for nanometer tech-

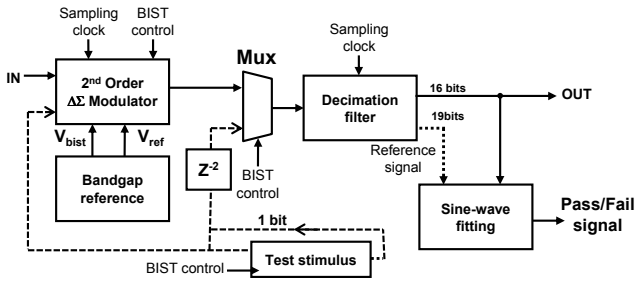

Fig. 2. BIST technique under evaluation.

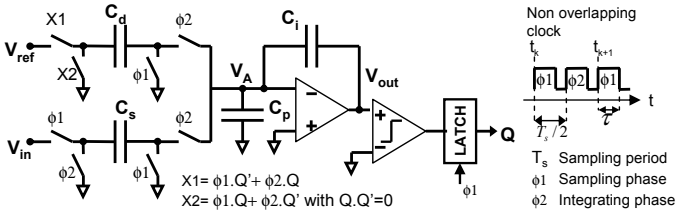

Fig. 3. First-order SC ΣΔ modulator.

nologies for which analog design is becoming ever more difficult due to reduced power supplies. In addition, ΣΔ modulation shapes the conversion quantization noise out of the frequency band of interest. The block-level schematic of a second order ΣΔ ADC is shown in Fig. 1. As is common in the analysis of ΣΔ ADC, we assume that the modulator output is filtered by a brick-wall filter with a gain of 1 in the signal band and 0 elsewhere. Testing ΣΔ modulators is a costly task due to the need of generating a high precision analog test signal and the requirement to acquire a large number of output digital samples. To this end, a promising BIST technique has been presented in [8] that considers purely digital test stimuli and largely simplifies the on-chip implementation of the sine-wave fitting algorithm. The reader is referred to [8] for a comprehensive overview of BIST techniques proposed to date for ΣΔ ADCs.

A. BIST Technique Under Evaluation

In this work, we evaluate the technique in [8] in terms of the resulting test metrics. The technique aims to measure the SNDR performance of switched-capacitor (SC) ΣΔ modulators. The test stimulus is an analog sinusoidal signal encoded as a binary stream with a 19-bit precision and stored into a digital linear feedback shift register. As shown in Fig. 2, this digital stimulus is first sent directly to the decimation filter in order to provide a high precision digital reference signal. Next, it is sent to the modulator which is now connected to the decimation filter via the multiplexer. In this step, the digital stimulus is converted and attenuated by an 1-bit Digital-to-Analog Converter (DAC) using voltages V_{bist} and V_{ref} that are provided by a bandgap generator already existing in the modulator. Since the signal undergoes a delay of two clock periods through the modulator, a z^{-2} delay block is considered during the generation of the reference signal. This way, the response of the converter to the test stimulus is synchronized with the reference signal. As a result, no phase response needs to be calculated by the sine-wave fitting algorithm, and the response analysis resources are largely simplified.

The modulator is implemented in an 0.13 μm CMOS technology and it is suitable for audio converter applications that must have 16 bits of resolution or, equivalently, an output SNDR of at least 96 dB. Silicon results show that excellent correlation is obtained between the embedded self-test and a sinusoidal standard test, resulting in an SNDR error smaller than 1 dB. However, since the converter cannot be stimulated with a full scale analog signal encoded in the bit stream, the capability of the BIST technique to detect all types of parametric deviations remains to be demonstrated. In particular, parametric deviations that induce small signal distortions may be hard to detect with test signals that are not full scale.

B. Behavioral model of first-order SC ΣΔ Modulator

This section presents a time-domain behavioral model of a first-order SC ΣΔ modulator (MOD1) following the approach proposed in [13]. Fig. 3 shows the circuit schematic along with the clock signals that activate the switches within an interval $[t_k, t_{k+1}]$ of length $T_s = 1/f_{clk}$, where f_{clk} is the clock frequency. To compute the integrator's output response at each clock period, we consider the main nonidealities of the operational amplifier (finite open-loop gain A_0, finite unity gain frequency ω_t, slew-rate SR, saturation levels, input parasitic capacitance C_p and thermal noise) as well as the variation of the gains of the signal path $G_1 = C_s/C_i$ and of the feedback $G_2 = C_d/C_i$. The input signal v_{in} is slowly varying such that within a clock interval it does not change appreciably, i.e $v_{in}(t) = v_{in}(t_k)$, for $t \in [t_k, t_{k+1})$. Without loss of generality, consider $Q = 0$. The integrator's output at each integration phase involves taking into account the charge sampled in the different capacitors during phase ϕ_1 and then applying the charge conservation at node A after $\phi_2 \rightarrow 1$. At $t \in [t_k + T_s/2, t_k + T_s/2 + \tau)$ we have

$$\begin{aligned} C_t v_A(t) - C_i v_{out}(t) = \\ -C_s v_{in}(t_k) - C_d V_{ref} + (C_p + C_i) v_A(t_k) - C_i v_{out}(t_k) \end{aligned} \quad (6)$$

where $C_t = C_s + C_d + C_i + C_p$.

In addition, we assume a single-pole amplifier model

$$-v_A(t) = \frac{v_{out}(t)}{A_0} + \frac{1}{\omega_t} \cdot \frac{dv_{out}(t)}{dt}. \quad (7)$$

Combining (6)-(7), we obtain a first-order differential equation of the integrator output

$$\begin{aligned} \frac{C_t}{\omega_t} \cdot \frac{dv_{out}(t)}{dt} + \left(\frac{C_t}{A_0} + C_i \right) v_{out}(t) = \\ C_s v_{in}(t_k) + C_d V_{ref} \\ + \left(\frac{C_i + C_p}{A_0} + C_i \right) v_{out}(t_k) \\ + \frac{C_i + C_p}{\omega_t} \cdot \frac{dv_{out}(t)}{dt} \Big|_{t = t_k + T_s/2}. \end{aligned} \quad (8)$$

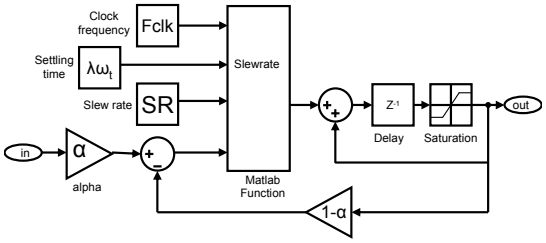

Fig. 4. Real integrator behavioral model.

The complete solution of (8) is given by:

$$v_{out}(t) \approx \alpha v_{out}(t_k) + \alpha v_s(t_k)\left(1 - e^{-\lambda\omega_t\cdot[t-(t_k+T_s/2)]}\right) \quad (9)$$

where

$$\lambda \approx \frac{C_i}{C_t}, \qquad \alpha \approx \frac{C_i A_0}{C_t + C_i A_0}, \quad (10)$$

and

$$v_s(t_k) = G_1 v_{in}(t_k) + G_2 V_{ref}. \quad (11)$$

Repeating the analysis for $Q = 1$, the complete solution rests the same apart from a change in the sign of V_{ref} in (11). Thus, we can simply write $v_s(t_k)$ as

$$v_s(t_k) = G_1 v_{in}(t_k) + G_2 V_{ref}(\bar{Q} - Q). \quad (12)$$

1) Finite A_0: The consequence of the finite open-loop gain of the amplifier is that only a fraction α of the previous output of the integrator is added to each new input. Setting $\omega_t \to \infty$ in (9), we obtain the transfer function $H(z)$ in the z-domain

$$H(z) = \frac{V_{out}(z)}{V_s(z)} \approx \alpha \frac{z^{-1}}{1 - \alpha z^{-1}}. \quad (13)$$

2) Finite ω_t and SR: The finite ω_t and the *SR* result in an incomplete or inaccurate charge transfer to the output node at the end of each clock cycle. Recall that the evolution of the output of the integrator within the $(k+1)$ integration period is given by (9). The slope of $v_{out}(t)$ reaches its maximum value at $t = t_k + T_s/2$

$$\left.\frac{dv_{out}(t)}{dt}\right|_{\max} = \lambda\omega_t\alpha v_s(t_k). \quad (14)$$

If $SR > \lambda\omega_t\alpha v_s(t_k)$, then there is no *SR* limitation and the output at the end of the integration period is given by

$$v_{out}(t_{k+1}) = \alpha v_{out}(t_k) + \alpha v_s(t_k)\left(1 - e^{-\lambda\omega_t\tau}\right). \quad (15)$$

If $SR < \lambda\omega_t\alpha v_s(t_k)$, then the operational amplifier is slewing until $t = t_0 > t_k + T_s/2$, at which point the slope of $v_{out}(t)$ becomes equal to *SR*. Thus,

$$v_{out}(t) = v_{out}(t_k) + SR\cdot t,\ t \in [t_k, t_0]. \quad (16)$$

For $t \in [t_0, t_k + T_s/2 + \tau]$, equations (6) and (7) are valid by replacing t_k with t_0 (notice that $v_{in}(t_0) = v_{in}(t_k)$). A similar analysis as before yields

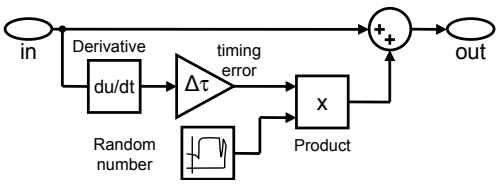

Fig. 5. Clock jitter behavioral model.

$$v_{out}(t) \approx v_{out}(t_0) + (\alpha v_s(t_k) - SR\cdot t_0)\left(1 - e^{\lambda\omega_t\cdot[t-t_0]}\right). \quad (17)$$

Imposing the continuity of the derivatives of equations (16)-(17) at $t = t_0$, we obtain the value of t_0

$$t_0 = \frac{\alpha v_s(t_k)}{SR} - \frac{1}{\lambda\omega_t}. \quad (18)$$

Clearly, if $t_0 > t_k + T_s/2 + \tau$, equation (16) holds for the whole clock period.

Fig. 4 shows the behavioral model of the real integrator which implements the transfer function $H(z)$ and the equations (15)-(18).

3) KT/C and Operational Amplifier Thermal Noise: The main noise sources are the KT/C noise associated with the on-resistance of the sampling switches and the intrinsic noise of the operational amplifier. The noise is accumulated at each period in the integrating capacitor. The equivalent noise power at the input of the integrator is given by [14]

$$\overline{v_n^2} = \frac{2KT_c\Theta_s}{C_s} \quad (19)$$

where K is the Boltzmann constant, T_c is the temperature,

$$\Theta_s = 1 + \frac{C_d}{C_s} + \lambda\omega_t\left(R_s C_s + R_d\frac{C_d^2}{C_s} + R_\alpha\frac{(C_s+C_d)^2}{2C_s}\right), \quad (20)$$

R_α is the equivalent input noise resistance of the amplifier and R_s, R_d are the on-resistances of the sampling and feedback switches, respectively. The flicker noise contribution was not modeled because there exist design techniques that cancel its effect with respect to the thermal noise. Depending on the converter application, flicker noise can be modeled as discussed in [15].

4) Clock Jitter: Clock jitter results in a nonuniform sampling time sequence. The introduced error depends on the statistical properties of the jitter as well as the input signal. Let $\delta(t_k)$ be the timing error at sampling point t_k. Assuming a sinusoidal input signal of frequency f_{in}, the error is given by

$$v_{in}(t_k + \delta(t_k)) - v_{in}(t_k) \approx \delta(t_k)\left.\frac{dv_{in}(t)}{dt}\right|_{t=t_k}. \quad (21)$$

Typically, it is assumed that δ follows a zero mean normal distribution with standard deviation $\Delta\tau$. The effect of clock jitter can be simulated at the behavioral level using the block in Fig. 5.

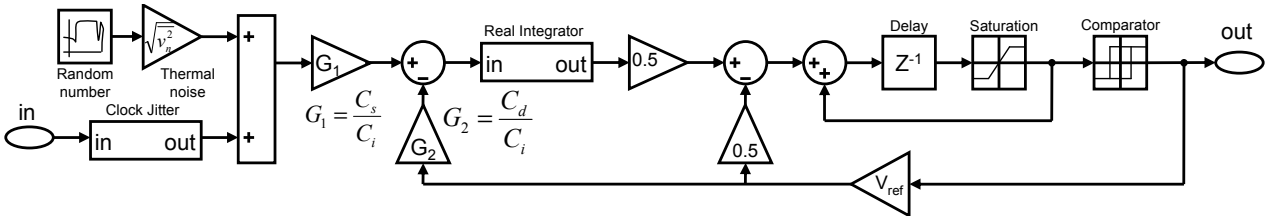

Fig. 6. Low-pass second-order ΣΔ modulator model.

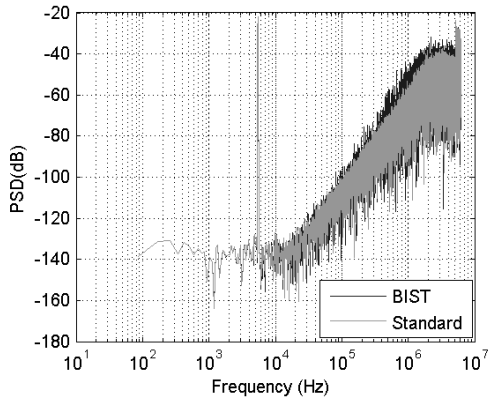

Fig. 7. Modulator output spectrum.

C. Behavioral model of second-order SC ΣΔ Modulator

The behavioral model of the second-order SC ΣΔ modulator (MOD2) is constructed based on the behavioral model of MOD1, as shown in Fig. 6. An ideal second stage is included betweeen the first integrator and the comparator. Only the nonidealities of the first stage are considered since most nonidealities in the second stage are attenuated due to noise shaping [13]. The total noise and clock jitter are superimposed to the input voltage. In summary, the vector B comprises 14 parameters, namely A_o, ω_t, SR, positive and negative saturation levels, C_i, C_s, C_d, C_p, R_α, R_d, R_s, jitter, and comparator's offset. The complete model is built and simulated in MATLAB SIMULINK. A single behavioral simulation to calculate SNDR lasts about 3 sec on an Intel Core2 2.40-GHz PC. Fig. 7 shows the FFT of the output bit stream of the behavioral model for two type of inputs, a perfect analog sinusoidal (standard test) and a high resolution digital sinusoidal encoded in a bit stream (BIST).

D. Extraction of $B^0_{n\times N_B}$

The initial population $B^0_{n\times N_B}$ of behavioral parameters is extracted from transistor level simulation. Certain behavioral parameters require special test benches. This section aims at describing the different test benches used for the simulation.

1) A_0, ω_t, and capacitors: The standard test bench for measuring A_0 has an open-loop configuration and will not work in the presence of mismatch because the equivalent input DC offset V_{off} will often saturate the outputs, thus resulting in erroneous values for A_0 and ω_t. To tackle this problem, we have used the test bench of Fig. 8. In this case, the DC differential output voltage is forced to be zero without affecting the calculation of A_0 and ω_t. In addition,

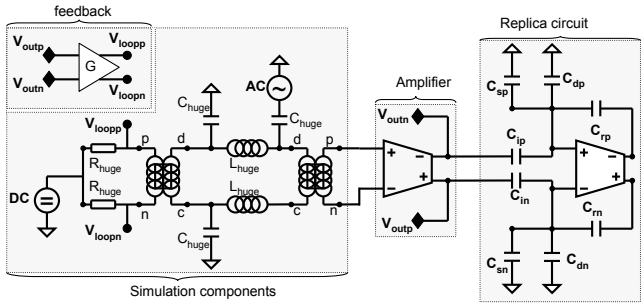

Fig. 8. Test bench in the presence of mismatch.

we consider a replica of the integrator in order to emulate the application environment and to obtain at the same time the variation in the values of capacitors.

2) Noise: As mentioned in section IV-B.3, the intrinsic noise within the operational amplifier is translated to an equivalent input noise resistance R_α. To calculate R_α, we use the precedent test bench with the AC source replaced by a noise source. The resulting value is

$$R_\alpha = \frac{\overline{v^2_{n,amp}}}{4KT_c} \tag{22}$$

where $\overline{v^2_{n,amp}}$ denotes the mean square input-referred amplifier noise voltage computed over its frequency band (100kHz-100MHz). R_s and R_d in (20) are extracted using a simple DC analysis.

3) SR: To compute the *SR*, the amplifier is configured in open-loop and is set to its maximal negative differential output voltage (we consider only the rise time). A step is then applied at the input in order to invert the output state of the amplifier. The time spent between 10% and 90% of the final output value is used to compute *SR*.

4) Jitter: We assume a clock jitter with zero mean and standard deviation $\Delta\tau = 200psec$.

5) Comparator offset: The offset is simply the differential output of the comparator when it is configured in closed-loop with unity gain.

V. Test Metrics Estimation

The experiment is carried out with $n = 10^3$, $n' = 10^4$ and $N = 10^6$ (see section III). In our case, $P = p_1$ is the standard SNDR measurement, which uses a sinusoidal of amplitude equal to the full dynamic range, and $M = m_1$ is the SNDR computed using the binary stream as test stimulus. The specification limit is set at 96 dB, that is the converter must have at least 16 bits of resolution. However, the BIST binary

stimulus has a lower amplitude in order to avoid overloading the modulator as discussed in the introduction of section IV, which makes the corresponding test limit lower by 12 dB. Therefore, the events C_g and T_p occur when $p_1 > 96$ dB and $m_1 > 84$ dB, respectively. The elapsed time to obtain the density estimate $f_B(B)$ and to generate $N = 10^6$ samples from it using MATLAB was approximately 25 minutes on an Intel Core2 2.40-GHz PC. The mappings $g_1 : B \mapsto p_1$ and $g_2 : B \mapsto m_1$ can be trained using a Feed Forward Neural Network (FFNN) in a few minutes and have a mean absolute error of less than 0.5 dB when they are used to predict the SNDR of new devices.

The resulting test metrics estimates are $T_E = 1.16\%$ and $Y_L = 0.73\%$ using the proposed technique. These values are at first glance unacceptable, which implies that the BIST technique cannot replace the standard test without affecting test accuracy. Notice that the design yield is estimated to be $Y = 98.37\%$, thus about 30% of devices with excessive parametric deviations causing performance failure are detected.

The method allows us to explain the obtained test metrics. In particular, we can use the large population $B^1_{N\times N_B}$ of one million devices to uncover trends in the behavioral-level parameters of circuits that give rise to T_E and Y_L. Our findings show that the most influential behavioral-level parameters are ω_t and the gains G_1, G_2. Specifically, we noticed that test escape is a consequence of having a low ω_t. In this case, the settling time $\lambda\omega_t$ is small affecting significantly the integration of the analog input sinusoidal (standard test) and, thereby, resulting in $p_1 < 96$ dB. In contrast, this effect is less apparent for the binary input stimulus (BIST) since the sampled voltage values are always the same. In this case, m_1 remains well above the test limit of 84 dB, thereby resulting in false acceptance. If we eliminate the devices with low ω_t from $B^1_{N\times N_B}$, it turns out that $Y = 99.81\%$, $T_E = 0.25\%$, and $Y_L = 0.17\%$. Moreover, we noticed that yield loss is primarily due to large positive deviations of G_1 and G_2. In fact, we considered global (instead of local) capacitor mismatches, which have resulted in a rather unrealistic value for the gains G_1 and G_2. High gains cause an overload of the modulator, which in turn reduces its capability to shape the noise out of its bandwidth. In this case, m_1 becomes too pessimistic, thus giving rise to yield loss. After eliminating the devices with large G_1 and G_2, the test metrics turn out to be $Y = 99.93\%$, $T_E = 0.069\%$, and $Y_L = 0.005\%$.

VI. Conclusion

In this paper, we have proposed a complete method to evaluate test techniques at the design stage for complex, hard-to-simulate circuits. The underlying idea is to develop a statistical model of the circuit under test, which can be simulated very fast. Thereafter, a large volume of data is generated which can be used to estimate test metrics with parts per million accuracy. To achieve this, we use a combination of behavioral modeling, density estimation, and regression. The method is demonstrated on a BIST technique for ΣΔ ADCs and allows us to pinpoint the combination of behavioral-level parameters that give rise to parametric test escape and yield loss. Future work will aim to study if these behavioral-level parameter combinations are realistic for the case of a robust design. Eventually the BIST technique might need to be refined based on these observations. Furthermore, we are planning to use the method in order to compare the array of different test techniques proposed to date for ΣΔ ADCs, thus providing guidelines about the feasibility of the approaches.

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