Error-Tolerance

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Because of trends in scaling, in the near future every high performance dice will contain a massive number of defects and process aggravated noise and performance problems. In an attempt to obtain useful yields, designers and test engineers will need to adopt a qualitatively different approach to their work. They will need to learn, enhance and deploy techniques such as fault- and defect-tolerance. For some applications, they may even apply error-tolerance, a somewhat controversial emerging paradigm. A circuit is **error-tolerant (ET)** with respect to an application, if (1) it contains defects that cause internal and may cause external errors, and (2) the system that incorporates this circuit produces *acceptable results*. In this presentation we illustrate and give quantitative bounds on several factors that will shape the future of digital design. We compare and contrast defect and fault-tolerant schemes with that of error-tolerance. We discuss how yield can be optimized by appropriately selecting the granularity of spares in light of defect densities and interconnect complexity. Finally, we show that several large classes of consumer electronic applications are resilient to errors, and how error-tolerance can then be used to significantly enhance effective yield.

Biography

Melvin A. Breuer received his Ph.D. in electrical engineering from the University of California, Berkeley, and is the Charles Lee Powell Professor of Electrical Engineering and Computer Science at the University of Southern California. He was Chairman of the Department of Electrical Engineering-Systems from 1991-1994, and again from 2000-2003. He was Chair of the Faculty of the School of Engineering, USC, for the 1997-98 academic year. His main interests are in the area of computer-aided design of digital systems, design-for-test and built-in self-test, and VLSI circuits.

Dr. Breuer is the editor and co-author of **Design Automation of Digital Systems: Theory and Techniques**, Prentice-Hall; co-author of **Diagnosis and Reliable Design of Digital Systems**, Computer Science Press; and co-author of **Digital System Testing and Testable Design**, Computer Science Press 1990 and reprinted in 1995 by the IEEE Press. He has published over 220 technical papers and was formerly the editor-in-chief of the *Journal of Design Automation and Fault Tolerant Computing*, on the editorial board of the *Journal of Electronic Testing*, and the co-editor of the *Journal of Digital Systems*. He was co-author of a paper that received an honorable mention award at the *1997 International Test Conference*, and the co-author of the best paper at the 2000 Asian Test Symposium. He is a Life Fellow of the IEEE; was a Fulbright-Hays scholar (1972); received the 1991 Associates Award for Creativity in Research and Scholarship from the University of Southern California, the 1991 USC School of Engineering Award for Exceptional Service, the IEEE Computer Society's 1993 Taylor L. Booth Education Award, an Okawa Foundation Research (2003), and the first (2000) Engineering Faculty Council Award for Outstanding Meritorious Service to the USC School of Engineering. He was the keynote speaker at the Fourth Multimedia Technology and Applications Symposium, 1999, and the Ninth Asian Test Symposium, 2000.