

A Novel Low-Power Scan Design Technique Using Supply Gating

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Abstract—Reduction in test power is important to improve battery life in portable devices employing periodic self-test, to increase reliability of testing and to reduce test-cost. In scan-based testing, about 80% of total test power is dissipated in the combinational block. In this paper, we present a novel circuit technique to virtually eliminate test power dissipation in combinational logic by masking signal transition at the logic inputs during scan shifting. We realize the masking effect by inserting an extra supply gating transistor in the VDD to GND path for the first level cells at output of the scan flops. The supply gating transistor is turned off in the scan-in mode, essentially gating the supply. Adding an extra transistor in only one logic level renders significant advantage with respect to area, delay and power (in normal mode of operation) overhead compared to existing methods, which use gating logic at the output of scan flops. Simulation results on ISCAS89 benchmarks show upto 79% improvement in area, upto 32% in power (in normal mode) and upto 7% in delay compared to lowest-cost known alternative.

I. INTRODUCTION

Power dissipation during test mode can be significantly higher than during functional mode, since the input vectors during functional mode are usually strongly correlated compared to statistically independent consecutive input vectors during testing. Zorian in [1] showed that the test power could be twice as high as the power consumed during the normal mode. Test power is an important design concern to increase battery-life in hand-held devices, that incorporates BIST circuitry for periodic self-test. It is also important to improve test-cost, since reduced test power of a module allows parallel testing of multiple embedded cores in an IC [5]. Peak and average power reduction during test is also important to improve reliability of test and improve yield [9]. It is, thus, important on the part of the designer to ensure reduction in power dissipation during the test mode.

Scan architectures represent prevalent Design for Testability (DFT) approach to test digital circuits [7]. During testing in a scan-based circuit, power dissipation occurs in both the sequential scan elements and in the combinational logic. While scan values are loaded into a scan chain, the effect of scan-ripple propagates to the combinational block and redundant switching occurs in the combinational gates during the entire scan-in period. It is observed that about 78% of total test energy is dissipated in the combinational block alone [8]. Hence, a low-power scan design should address techniques to reduce power dissipation in the combinational block.

There has been multitude of research exploring efficient techniques to reduce test power in scan-based circuits. Wang

et. al. proposed automatic test pattern generation technique to reduce power dissipation during scan testing [4]. With their ATPG, redundant transitions in combinational logic can be reduced but not completely eliminated. Whetsel in [5] provided a solution for average and peak power dissipation by transforming conventional scan architecture into desired number of selectable, separate scan paths. Sankaralingam et al. proposed a solution to the peak power problem during external testing by selectively disabling the scan chain [6]. In [9] and [10], the authors provide a solution to prevent peak power violation during both shift and capture cycle using scan chain partitioning. Redundant power loss in combinational logic is reduced but not completely prevented in the above cases [4] [5] [6] [9] [10], since part of the scan chain is always active during shifting.

Inserting blocking logic into the stimulus path of the scan cells (as shown in Fig. 1) to prevent propagation of scan-ripple effect to logic gates offers a simple and effective solution to significantly reduce test power, independent of test set. Werstendorfer et. al. has proposed NOR or NAND gate-based blocking method in [8]. Blocking gates (of type NOR or NAND) are controlled by the test enable signal and the stimulus paths remain fixed at either logic 0 or logic 1 during the entire scan shift operation. Zhang et. al. have used multiplexers at the output of the scan cells, which holds the previous state of the scan register during shifting [11]. Another method for reduction in combinational power using blocking is to use a scan-hold circuit as a sequential element. This technique is called *enhanced-scan* [7], which also helps in delay fault testing by allowing application of two-pattern test. In a scan-hold design, each sequential element contains an additional storage cell named *hold* latch and stimulus path for combinational part is connected to the output of the hold latch, which is not used in scan shifting. Therefore, it also prevents redundant switching in combinational logic.

The problem with the blocking logic is that, they add significant delay in the signal propagation path from the D-FF to logic [8]. Moreover, they have large overhead in terms of area and switching power in normal operation of the circuit. In this paper, we present an elegant signal blocking technique, referred as First Level Supply gating or FLS, to reduce power dissipation in the combinational logic during scan shifting. This is achieved by selectively inserting a supply gating transistor in the first level of logic connected to the scan cell outputs, which essentially “gates” the ripple in scan-latches.

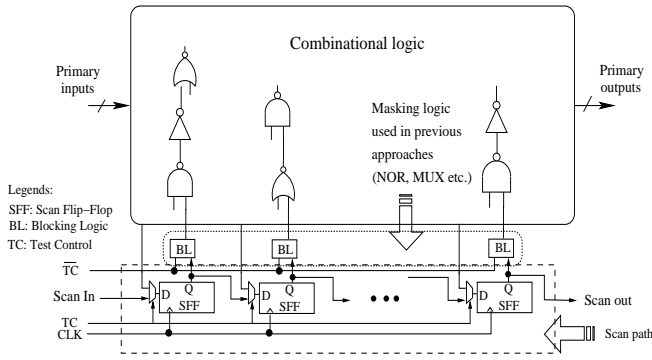


Fig. 1. Existing gating circuitry to reduce power during scan operation

Transistor gating technique, which effectively gates the VDD or GND line, has been widely used for reducing leakage due to the stacking effect [2] [3]. To the best of our knowledge, it has never been used to save active power in a circuit. We have used it, in a novel way, to save active power in the combinational logic during scan shifting. The proposed method is as effective as the other blocking methods in terms of reducing peak power and total energy dissipation during scan testing. But since we introduce just one transistor in the discharge path of the first level logic, the delay penalty is significantly reduced over other blocking methods, which insert additional level of logic into signal propagation path. The overhead incurred in die-area and switching power in normal mode of operation due to extra DFT logic are also significantly lower than the methods using NOR, MUX, and Hold-latch.

The rest of the paper is organized as follows: Section II illustrates the proposed gating technique for saving energy in the combinational block during scan shifting. Section III presents experimental results in terms of area, delay, power for a set of benchmark circuits. Section IV describes important test issues associated with the proposed technique. Section VI concludes the paper.

II. FIRST LEVEL SUPPLY GATING FOR POWER REDUCTION IN SCAN MODE

The dynamic power dissipation in the combinational circuit can be reduced by lowering the activity of the circuit. Previous works target to reduce the activity of the circuit by gating the input of the combinational block with the use of extra logic gates (latch [7], multiplexer [11], NOR [8], etc.). However, these techniques have a negative impact on circuit performance and considerably add to the total area. Moreover, they impose significant power overhead during the normal mode of operation of the circuit. In this section, we have described a novel methodology to reduce the power dissipation in the combinational circuit during the scan shift cycle.

A. Supply Gating for Reducing Active Power in Scan Mode

In this paper, we propose to use the supply gating for dynamic power reduction by reducing the activity of the combinational block during scan shift. To understand how supply gating can be used to reduce the dynamic power, let us consider the inverter chain shown in Fig. 2. Let us consider

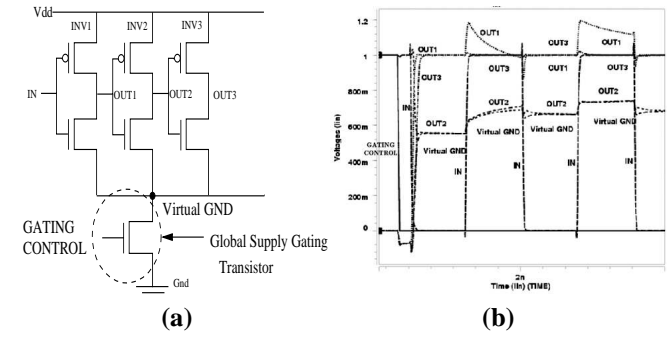


Fig. 2. (a) Use of global supply gating transistor in combinational part; (b) Transient response in 70nm

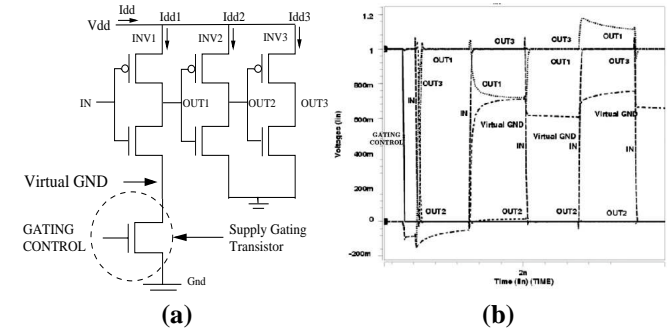


Fig. 3. (a) Use of first level supply gating transistor in combinational part; (b) Transient response in 70nm

that a NMOS supply gating transistor is used in series with the pull-down NMOS of the inverters. In Fig. 2(a), the supply gating transistor is shared by all the inverters in the chain (global supply gating). Let us now consider that before the application of the SLEEP signal (i.e. before turning off the supply gating transistor) the input IN was stable at '1' and after application of SLEEP, the input IN switches from '1' to '0'. This will turn on the PMOS P1 of the inverter INV1 and the output OUT1 of INV1 will be charge to VDD. This will result in a '0' to '1' transition in the input of INV2. However, since the supply gating NMOS is off there is no discharge path for the output of INV2. Hence, OUT2 cannot fully discharge to 0, and rather it gets discharged to the virtual ground.

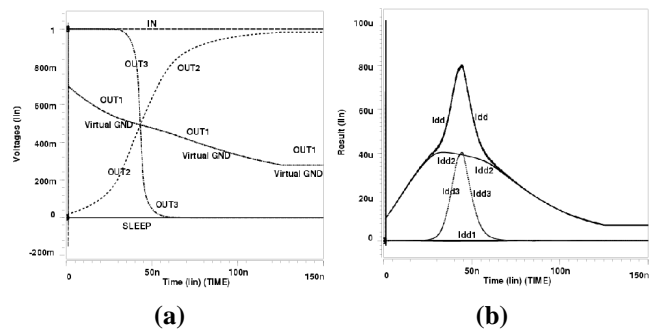


Fig. 4. Static short circuit issue in FLS (a) Transient voltage waveform for the circuit in 3; (b) Supply currents of inverters in the same circuit (simulated in 70nm)

The virtual ground voltage rises to some intermediate voltage due to charge sharing. As observed in Fig. 2(b) the output voltages of gates settle down in few cycles and therefore, the further switching at the input IN of the inverter chain cannot propagate. Moreover, if in the next cycle, there is '0' to '1' transition at the input IN, the output of INV1 cannot be discharged. Hence, at most only one switching (between '0' and '1') can occur (Fig. 2(b)). This drastically reduces the activity of the combinational logic during scan shift, thereby lowering the dynamic power.

As we have mentioned, the supply gating transistor can be used by the designer to reduce leakage power. The supply gating transistor can be either shared among all the gates in the logic (global supply gating) or it is distributed such that there is a separate supply gating transistor for each logic gate (distributed supply gating) [2] [3]. Thus, the global or distributed supply gating transistors introduced in a combinational block can be easily utilized to reduce the dynamic power dissipation during scan-shift. In this case, the reduction in the dynamic power is achieved without any new design overhead. The logic that controls the SLEEP signal in the normal mode of operation need to be AND-ed with the TEST-MODE signal to turn-off the supply gating transistor(s) during scan-shift. However, introduction of global or distributed supply gating transistors only for the reduction of power during scan-shift is not a viable option because, the use of a global supply gating transistor is associated with performance degradation [3]. To reduce the performance penalty, a large supply gating transistor is required. when a global supply gating transistor is inserted, it results in large area overhead. On the other hand, if it is distributed, then several of the smaller transistors will be required. Although this will reduce the performance penalty, but the total supply gating device width of the distributed approach will be higher than the global case. Also, distribution of supply gating transistor requires complex routing of the SLEEP signal which can significantly increase the routing area. Hence, it can be concluded that the introduction of the existing supply gating transistor techniques (used for leakage reduction) only for the TEST-MODE will have considerable performance degradation and area overhead.

To overcome the previously mentioned difficulties associated with the standard (global or distributed) supply gating technique, we have proposed a novel First Level Supply gating (FLS) insertion technique, where only the first level logic gates connected to the scan flops are gated using supply gating transistors (Fig. 3(a)). As explained earlier, insertion of the supply gating transistor in the first level logic will screen the rest of the combinational logic from the state-input (scan-input) transitions (except only one transition - a '1' to '0' if GND gating and '0' to '1' in VDD gating). This can be observed in Fig. 3(b). From this figure it can be understood that the first transition at the input IN from '1' to '0' will charge the OUT1 to VDD. This transition will propagate throughout the inverter chain. However, any further transition in the input (i.e. from '0' to '1') will not propagate, as the OUT1 cannot be discharged (Fig. 3(b)). This significantly reduces the redundant

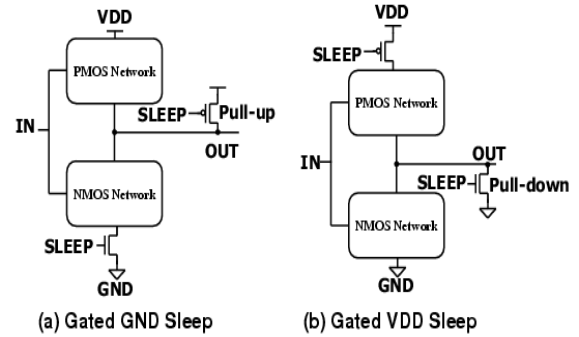


Fig. 5. Proposed supply gating schemes

activity of the circuit during the scan-shift operation.

The principal issue associated with FLS scheme shown in Fig. 3 is that the outputs of the first level gates are floating if they are at logic '0' (connected to the virtual ground). The voltage of a floated output is determined by the leakage balance between the pull-up PMOS and pull-down NMOS network of the gate. Moreover, crosstalk noise or transient effect due to soft error can easily change the voltage of a floated output. If the voltage of the output of a first level gate is not exactly at VDD or GND, this could cause static short circuit current on the following logic gates being driven by the first level gate. This particularly becomes more of an issue in deep submicron technologies due to increased leakage and noise. For example, let us assume the input of the inverter chain of Fig. 3 makes a '0' to '1' transition in the supply gating mode and stays at '1' for a long time. The voltages of the outputs of the inverter chain for this scenario are shown in Fig. 4(a). The OUT1 voltage decays and settles down at some intermediate voltage due to the leakage of the supply gating transistor. As OUT1 slowly decays below $V_{dd} - V_{th}$, in the second inverter, both the PMOS and NMOS transistors get turned ON causing static short circuit current flowing through the second inverter (I_{dd2} in Fig. 4(b)). Consequently, the output of the second inverter (OUT2) rises resulting in static current on the third inverter (I_{dd3}). If OUT1 decays below the trip point of the second gate, a switching also occurs on the second gate as shown in Fig. 4(a). As observed from Fig. 4(b), this could result in significant static short circuit current in the supply gating mode. Although the voltage rise/drop decrease as it propagates through the logic gates, the continuous flow of short circuit current in the gates at second stage could result in significant power dissipation, eliminating the benefit of gating.

In order to avoid such an issue, the outputs of the first level gates need to be enforced at VDD or zero in the supply gating mode. If the GND is gated as in Fig. 3, then the outputs of the first level gates can be enforced to VDD by a pull-up PMOS driven by the SLEEP signal. If the VDD is gated then the outputs of the first level gates can be forced to ground using NMOS pull-down transistors driven by the SLEEP signal. The general schemes of the proposed supply gating are shown in Fig. 5. In order to evaluate and compare these two schemes (Fig. 5(a) and Fig. 5(b)), they are applied to NAND and NOR

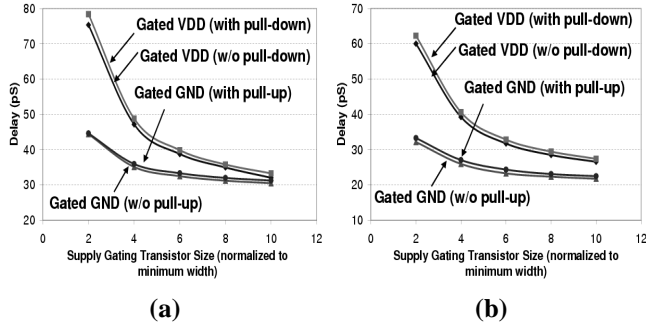


Fig. 6. Delay comparison of gated-VDD and gated-GND for (a) NOR gate and (b) NAND gate

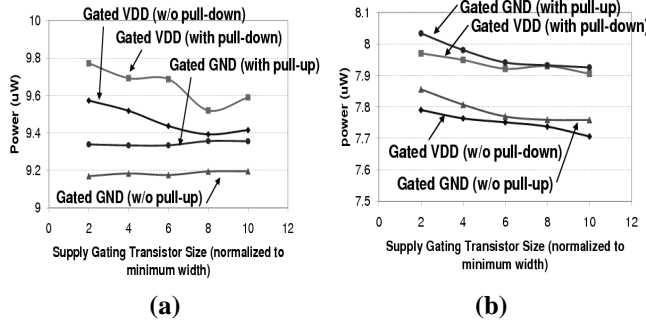


Fig. 7. Power comparison of gated-VDD and gated-GND for (a) NOR gate and (b) NAND gate

gates. The pull-up (pull-down) transistor is kept at minimum size to optimize its impact on circuit delay and power during normal mode of operation. Fig. 6 shows the delay comparisons of the gated-VDD and gated-GND circuits. As expected, for the same size of the supply gating transistor, the gated-GND circuit is faster than the gated-VDD circuit for both NOR and NAND gates. This is because NMOS transistors are faster than PMOS transistors at the same area. It is also observed that as the size of the supply gating transistor is increased the delay of the circuit is reduced and gets closer to the delay of the circuit without any gating. However, increasing the transistor width for the supply gating transistor does not help much for delay improvement after some point. As observed from the plots in Fig. 6, for 2-input NAND and NOR gates, a supply gating transistor of 6 times the minimum size is a reasonable choice for minimal delay impact and small area overhead. Another point observed from Fig. 6 is that the impact of pull-up (pull-down) transistor on delay is negligible. Fig. 7 shows the power comparisons in the active mode for both the NAND and NOR gates. For the NAND gate there is not much difference in the power of the gated-VDD and gated-GND cases; however, for the NOR gate the gated-GND circuit shows less power consumption. From these results, it can be inferred that the gated-GND is a more suitable technique for gating due to smaller area overhead and less delay and power penalties.

B. FLS Scan Test Scheme

Fig. 8 shows the proposed FLS gating techniques applied to a general circuit. For the implementation of the supply

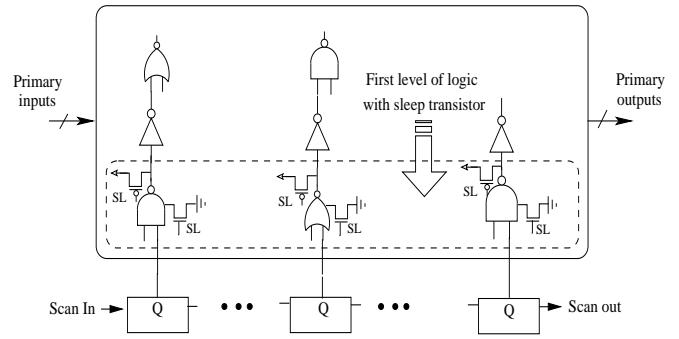


Fig. 8. Low power FLS scan test scheme

gating transistors in the FLS technique, two approaches can be taken: a) in one case the first level gates have separate supply gating transistors (Unshared FLS), and b) in the other case all first level gates share a single supply gating transistor (Shared FLS). By sharing the supply gating transistor, area overhead can be reduced because a shared supply gating transistor can have less size than the sum of the sizes of all supply gating transistors in the unshared case. In the unshared FLS, the size of the supply gating transistor is chosen to be 10 times the minimum transistor size, regardless of the type of the gate ($W_{supplygating} = 10 * W_{min}$). Statistically speaking, for random input data patterns, at each time approximately half of the first level gates are switching, while the rest do not experience any switching. Therefore the supply gating transistors of the idle gates are not actually used. Therefore, the size of the supply gating transistor in the shared FLS can be half the sum of the sizes of all supply gating transistors in the non-shared FLS. Based on this argument, the size of the supply gating transistor in the shared FLS case is given by:

$$W_{supplygating} = 0.5 * Fanout * (10 * W_{min}) \quad (1)$$

where, $Fanout$ is the number of first level gates in the combinational circuit. Therefore, by supply gating transistor sharing the area overhead due to supply gating transistor is reduced by half.

III. EXPERIMENTAL RESULTS AND COMPARISONS

To estimate the effectiveness of the FLS scheme, we simulated a set of ISCAS89 benchmark circuits and obtained power and performance in normal mode of operations and area overhead in case of FLS, NOR-based, MUX-based, and latch-based gating. The simulation was performed in the 70nm BPTM models [12] to observe the effect of gating in a sub-100nm scaled technology. The gate-level netlists were first technology-mapped to *LEDA* 0.25 μ standard cell library using Synopsys design compiler. The library contains complex gate types e.g. ‘‘aoi’’ (and-or-invert) and ‘‘mux’’, and hence, the total number of logic gates is reduced from that in original benchmark. The benchmark circuits are then translated to *Hspice* and scaled to 70 nm. Power is measured in *NanoSim* by applying 100 random vectors to the inputs and delay is measured by *Hspice* simulation of the critical paths of a circuit. Table I to III show comparisons of the proposed gating techniques with the conventional techniques.

TABLE I
COMPARISON OF PERCENTAGE AREA INCREASE

ISCAS89 Ckt	# Flops (Logic gates)	# Fanouts (Ratio)	% of area increase with					Improv over Nor (%)
			Latch gating	Mux gating	NOR gating	FLS (Unshared)	FLS (Shared)	
S298	14 (56)	35 (2.5)	15.10	13.74	6.86	6.55	3.57	47.91
S344	15 (63)	32 (2.1)	14.83	13.49	6.74	5.49	3.00	55.55
S641	19 (97)	19 (1.0)	14.24	12.95	6.47	2.47	1.35	79.17
S838	32 (123)	96 (3.0)	14.35	13.05	6.52	7.47	4.08	37.50
S1196	18 (247)	23 (1.3)	8.17	7.43	3.71	1.81	0.99	73.38
S1423	74 (303)	160 (2.2)	15.07	13.71	6.85	5.66	3.08	54.95
S5378	179 (600)	280 (1.6)	15.67	14.25	7.12	4.26	2.32	67.41
S9234	211 (823)	445 (2.1)	14.98	13.62	6.81	5.48	2.99	56.06
S35932	1728 (4876)	2692 (1.6)	16.80	15.28	7.64	4.54	2.48	67.54

TABLE II
COMPARISON OF DELAY (NORMALIZED TO SCALE OF 100)

ISCAS89 Ckt	Crit-path logic levels	Original Delay	Latch gating	Mux gating	NOR gating	FLS (Unshared)	FLS (Shared)	Improv over NOR (%)
s298	8	17.92	20.63	21.87	19.27	18.16	18.16	5.8
s344	11	22.27	24.64	25.48	23.33	22.23	22.23	4.7
s641	22	45.86	48.56	50.07	47.67	46.26	46.26	3.0
s838	20	47.56	49.76	50.35	48.39	47.75	47.75	1.3
s1196	16	34.62	37.25	38.76	35.78	34.78	34.78	2.8
s1423	46	95.51	98.28	100.0	97.05	95.94	95.94	1.1
s5378	13	26.73	29.04	29.79	27.68	26.72	26.72	3.4
s35932	14	17.07	19.78	21.18	18.59	17.30	17.30	7.0

TABLE III
COMPARISON OF POWER DURING NORMAL MODE OF OPERATION (NORMALIZED TO SCALE OF 100)

ISCAS89 Ckt	Original Power	Latch gating	Mux gating	NOR gating	FLS (Unshared)	FLS (Shared)	Improv over NOR (%)
s298	0.47	0.91	0.80	0.64	0.49	0.48	24.8
s344	0.55	1.00	0.87	0.59	0.57	0.56	4.0
s641	0.44	1.04	0.88	0.53	0.46	0.45	15.2
s838	0.74	1.86	1.56	1.29	0.94	0.98	24.1
s1196	1.83	2.41	2.28	1.89	1.84	1.84	2.4
s1423	2.96	5.35	4.87	4.36	2.73	2.97	31.8
s5378	5.61	10.74	9.27	6.28	5.44	5.68	9.6
s35932	50.35	100.00	83.82	58.26	46.72	47.99	17.6

Table I shows comparisons of these techniques in terms of area overhead. Since the layout rules for the 70nm node are not available, the measure used for area is the total transistor active area ($W * L$ for a transistor). As explained earlier, by supply gating transistor sharing in the Shared FLS case, the area overhead of the supply gating transistors can be reduced by half compared to the unshared FLS. The latch is the largest gating circuit and therefore the latch-based gating circuit has the largest area overhead followed by the MUX-based gating technique. The NOR-based gating has the least area penalty among the existing gating techniques. The proposed Shared FLS gating technique exhibit the smallest area overhead for all benchmark circuits (less than 10%). This technique shows 19% to 73% reduction in area overhead as compared to the conventional NOR-based gating technique which has the least area penalty among the alternative techniques.

Table II shows comparative impact of the conventional and proposed gating techniques on circuit delay for different

benchmark circuits. As observed from Table II, the proposed technique has the least impact (minimal increase) on circuit delay. The MUX-based gating has the largest increase in delay. The latch-based gating shows the second largest increase in delay and the NOR-based gating has the least delay penalty in conventional techniques. Compared to the NOR-based gating which has the least delay penalty in the conventional technique, the proposed gating technique exhibits delay reduction of up to 7%. In fact as observed from Table II, the delay overhead of the FLS technique is less than 1.5% for all the benchmark circuits. Another point to notice is that the delay of the NOR-based gating would be more if the input logic polarity is to be preserved. In that case, in the NOR-based gating an extra inverter need to be added to the inputs to correct the logic level. This further adds to the delay overhead of the NOR-based gating technique. Moreover, as the logic depth decreases for better performance in sequential circuit, the proposed FLS scheme will show much less delay overhead

as compared to the NOR-based gating. For example, assuming a logic depth of six composed of simple 2-input NAND and NOR gates, the delay overhead with the NOR-based technique is 19.6%, whereas this overhead in the FLS scheme is only 2.4%.

Table III shows comparisons of power in normal mode of operation. Significant power savings are observed for all the benchmark circuits. In fact, the power dissipation of the FLS circuits are very close to the power dissipation of the original combinational circuit without any gating techniques. This is because in the proposed technique, the supply gating transistor and the pull-up PMOS do not switch in the active mode. The only source of power overhead is due to the diffusion capacitance added to the outputs of the first level gates by the PMOS pull-up. However, this capacitance is negligible compared to the gate capacitance of the second level gates. It is interesting to notice that for large benchmark circuits such as s1423, s5378, and s35932 the power of the FLS circuit is even less than the power of the original circuit. This is due to the fact that the supply gating transistor results in leakage reduction (due to stacking [2]) for the idle gates. For the large circuits, at each time, there are many idle first level gates for any random pattern. The supply gating transistors reduce the leakage on the idle gates. In the 70nm technology node, the active leakage is a significant part of the overall active power. FLS shows power reduction of up to 32% compared to the NOR-based technique, as reported in the last column.

Our results indicate that the introduction of the proposed FLS technique has minimal overhead in terms of power, performance, and area while achieving a significant dynamic power reduction in the scan shift mode. As in the NOR-based gating [8], FLS allows at most two signal changes at a gated input for application of one test vector. Power saving result in test mode is, thus, expected to be similar to the ones reported in [8]. Larger-sized supply gating transistors for gates in the critical path can be used to further reduce the delay penalty. FLS does not require any additional control signal and the test control signal needs to be routed to the first level of logic instead of the scan flops as in standard scan design. Hence, the routing overhead in FLS is expected to be comparable to standard scan-based design.

IV. TEST ISSUES

Fault coverage and fault models remain unaffected with the insertion of FLS. During normal mode of operation the gating transistors are turned ON, hence, the conventional stuck-at fault models and delay fault models still remain valid. FLS does not require any change in test vectors generated by ATPG tools. Hence, we obtain the same fault coverage as before. However, insertion of extra transistors bring in the possibility of extra faults. Since the DFT overhead in our case is significantly lower than the MUX-based, NOR-based or enhanced-scan method, gating logic causes much lower impact on total fault set.

The proposed technique can be easily applied to scan-based test-per-scan BIST (Built In Self Test) [7]. A circuit

designed with BIST has weighted random pattern generator and output response analyzer built into the circuit. Random test patterns are generated by a Linear Feedback Shift Register (LFSR). The patterns are applied to both primary inputs and scan cells. Depending on how the test patterns are applied to the primary inputs (parallel or sequential like scan shifting), the combinational logic may suffer from redundant switching when the patterns are applied to primary inputs. In that case, we need to have masking logic for primary inputs too. FLS technique proposed for scan path can be equally used to the fanout logic gates for the primary inputs.

The proposed method also does not affect structural delay fault testing of the scan architecture. A test circuit with regular scan cells (not enhance-scan) is capable of performing delay tests where the second pattern is applied by switching only the primary inputs (broad-side delay testing) or by shifting the scan cells by one bit (skewed-load delay testing) [7]. In both cases, once the scan chain is loaded, we need to make the supply gating signal *high* to enable signal propagation and keep it at that level throughout the capture cycle.

V. CONCLUSIONS

This paper presents First Level Supply gating, which is a novel low-cost solution to prevent redundant switching in combinational logic during scan testing. Compared to existing methods using NOR or MUX-based output gating, the proposed technique can achieve similar saving in average and peak power during testing, while induces significantly lower DFT overhead with respect to die-area, circuit performance and power during normal operation. The technique maintains fault coverage and does not impact the test generation or test application process. It can be easily extended to apply in test-per-scan BIST and can be coupled with other scan-power reduction techniques like scan reordering or scan partitioning to produce additional saving in test power.

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