End-to-end testability analysis and DfT insertion for mixed-signal paths

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Abstract

Increasing system complexity and test cost demands new system-level solutions for mixed-signal systems. In this paper, we present a testability analysis and DfT insertion methodology for end-to-end mixed-signal paths. Based on behavioral models and path analysis, testability problems in the path are determined and classified in terms of their bottleneck. Possible solutions to each problem are identified. The DfT insertion problem is then formulated as a min-cost set cover problem to achieve the most cost-efficient solution. In experimental results where test point insertion is used as the DfT approach, nearly 50% reduction in the overall DfT overhead is achieved.

1 Introduction

Mixed-signal systems integrating digital and analog components are proliferating in the market. This trend is caused by the drive towards increased performance, enhanced functionality, and smaller size. While the functionality keeps increasing in typical mixed-signal systems, their market value and product life-time are decreasing, resulting in tighter profit margins and market windows. In order to survive this trend, low-cost solutions to design, manufacturing, and testing are needed. Manufacturing and design costs have recently reduced considerably thanks to innovative fabrication processes and design re-use and automation. However, the cost of testing mixed-signal systems has not reduced at the same rate, creating a significant burden.

Test methodologies developed for mixed-signal systems have traditionally focused on individual analog and/or mixed-signal modules, such as amplifiers, mixers, PLLs, rather than concentrating on system-level requirements. PLL jitter and data converter non-linearity have been the major focus of research over the last decade. In [1], an analytical signal method for PLL jitter measurement based on signal sampling and Hilbert transform [2] is presented. A delay-line based phase noise measurement method that uses a low intermediate frequency (IF) to overcome challenges due to increasing operation frequencies is presented in [3]. An oscillation-based DAC testing methodology is proposed in [4]. In the test mode, the DAC is configured in a closed-loop where its input is oscillated between two codes around a reference voltage.

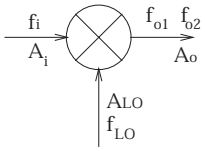
Methodologies proposed for test automation have also mostly focused on individual modules. Most automation efforts model the test development problem as a search for the *best test signal* within a constrained input space. Assuming a pure sinusoidal input, ideal test frequencies are determined through a binary search based on sensitivity information [5]. Similarly in [6], the search for test frequencies is conducted through maximizing the sensitivity of the target circuit component to the output signal.

System-level test approaches, on the other hand, focus on a specific application domain and aim at evaluation of a system-level performance parameter with the hope of exercising the worst case scenario. In order to extract a set of performance parameters for a transceiver path, a self-test strategy is presented in [7]. Unfortunately, most critical specifications, such as phase noise, blocker performance, and linearity, cannot be tested with this strategy as it would require duplication of the complicated signal interactions in the test data.

Recently, path-based test approaches have been proposed to concentrate on system-level capabilities while still using the well-understood module-level specifications [8, 9, 10]. The premise of path-based testing is the utilization of the functional signal path to provide test access to each of its constituent components. Behavioral models are used in test propagation through the signal path. The desired response is isolated from the undesired response during propagation by imposing certain restrictions on the test signal so as to prevent its corruption. Test quality can be evaluated through a statistical analysis taking the impact of noise and parametric variations into account [11].

While path-based test approaches promise low-cost system-level test solutions, in most cases, it is infeasible to test all specifications through the complete path [8]. The problem arises in cases where a subset of module-level parameters are specified through decomposition of a complex system-level parameter. In the case where the functional path proves to be insufficient to test such parameters, a DfT or BIST method is needed to ensure adequate test quality. However, if a distinct DfT solution is applied to each testability problem, the benefits of path-based testing may soon disappear. Clearly, a systematic way of analyzing path capabilities and testability problems is needed to determine a cost-efficient set of DfT solutions.

In this paper, we propose a testability analysis and DfT insertion methodology for path-based testing of mixed-signal systems. Through identification of system test capabilities and resulting testability problems, a set of possible solutions to each problem is determined. The lowest-cost



Model: $A_o = G_M * A_i$
$f_{o1} = f_i - f_{LO}$
$f_{o2} = f_i + f_{LO}$
Parameters: G_M, Phase delay
Non-ideal: Harmonic Bandwidth, Noise Figure, Isolation, IIP_3, P_{1dB}

Figure 1. Library Model of a Mixer

set of DfT solutions is the one that results in minimal hardware and performance overhead while providing adequate coverage for all parameters. Optimality can be achieved by considering each possible solution whereas computational tractability is ensured by the use of high-level models proposed in [8, 11], and early viability exploration.

2 Motivation

Specifications of a mixed-signal system can all be defined at the top level of hierarchy, theoretically requiring testing through only primary input and output. However, complex and hard to measure system specifications, such as RMS phase error, are typically decomposed into better-understood, module-level specifications, such as oscillator phase noise, amplifier DC offset, etc. As a result, a number of specifications may need to be measured at the module level generating a test access problem.

The goal of path-based test approaches is to solve such problems by using the functional signal path as a test access mechanism to each module in the path. In [8, 10, 11], a signal propagation framework has been proposed to enable path-based testing and to quantitatively evaluate test coverage using statistical analysis. While such a path-based approach has been proven to to reduce test access overhead and even test time, a subset of specifications typically remains untested through the complete path requiring the help of a DfT approach. In this paper, we primarily focus on providing a systematic approach for DfT insertion in the case where the complete path proves to be an insufficient test access mechanism. As the proposed testability analysis relies on the behavioral models introduced in [8], we provide an overview in this section.

Overview of behavioral models:
Even though analog circuits exhibit highly non-linear behavior, within a given operating range, the input-output behavior can be expressed with simple relations. The operating range where these linear relations hold can be limited by a number of attributes, such as frequency, amplitude, and number of tones. Outside the operating range, there exists a transition range where the circuit behavior is unpredictable and highly dependent on process variations. Finally, in the stop-band region, the circuit response is below the noise level and is assumed to be zero.

Each circuit generates a certain amount of noise and non-linear distortion. Moreover, parameter variations introduce an added level of uncertainty to signal attributes and need to be accounted for. Thus, such non-ideal behavior needs to be included in the behavioral models. As an example, the model of a mixer is shown in Figure 1.

3 Testability analysis and DfT Insertion

The proposed testability analysis and DfT insertion method is composed of five major steps, as shown in Figure 2. First, a path analysis is conducted to determine the testability problems in terms of the parameters that cannot be tested through the primary pinouts, together with their causes, such as noise, harmonic distortion, or parameter tolerance. Using this information, the set of modules that constitute the bottleneck for each problem can be determined. For example, if the testability problem arises from an inability to supply the required frequency or amplitude to a target module, then the modules that limit these ranges in the path can be identified as the bottleneck. This information helps in reducing the search space for possible DfT solutions that circumvent the bottleneck, such as a controllability point, false path, or BIST. Each testability solution results in a new system topology which needs to be re-evaluated since there may be secondary bottlenecks after the first level bottleneck is removed. This phase continues until at least one possible solution is identified for each testability problem.

In most cases, several types of DfT approaches, such as test point insertion or on-chip signal generation, may be identified within the overall set of possible solutions. Each DfT approach imposes various overheads in terms of area, capacitive loading, and the sensitivity of the circuit point being loaded. Moreover, each solution identified for the problem may provide a distinct level of test coverage. In order to minimize the overall overhead and maximize the test coverage, a selection methodology is needed. This problem is modeled as a min-cost set cover problem. A two-step approach is taken to achieve the most cost-efficient solution. First, an optimal algorithm based on integer linear programming [12] chooses the set of DfT solutions with minimal overhead. Next, a heuristic algorithm based on simulated annealing maximizes test coverage.

3.1 Path Analysis

In the mixed-signal domain, test requirements for a target specification can be defined in terms of a set of conditions on test signals. For example, the test input for the IIP_3 parameter needs to include at least two tones since it is related to intermodulation distortion. The power of each tone needs to be high enough to ensure that the weak response is observable yet low enough to prevent saturation. The cumulative noise level should not prevent the observation of the output response, and there should be no other

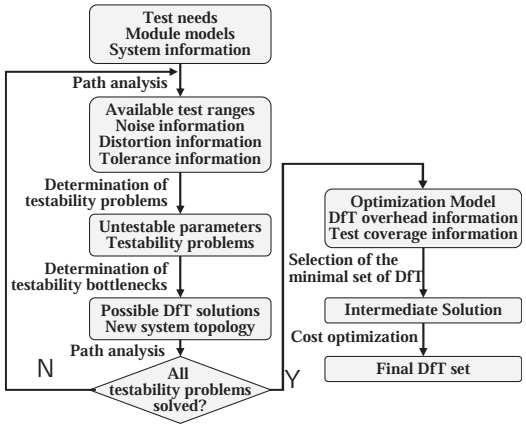


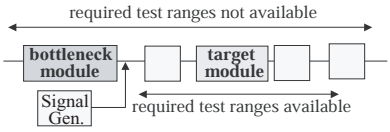
Figure 2. Proposed testability analysis and DfT insertion method

considerable third order distortion interfering with the test signal. Violation of any of these conditions may result in the corruption of test information, indicating a testability problem. In order to identify such problems, the nature of signals that can be propagated from the controllability point to the observability point through each module needs to be determined. A similar analysis is needed in the reverse direction, since test input and test response may not share the same attributes. The pieces of information that need to be tracked during path analysis consist of frequency range, amplitude range, number of signal tones, cumulative noise level, cumulative tolerance, and harmonic distortion. At the controllability point, the traversal starts with the capabilities of the tester. As each module is traversed, it imposes certain restrictions on the signal range, generates noise and distortion, and increases tolerance. Once the traversal is complete, test needs of each module are compared with the signal attributes that can be provided to that module through the given path. At this point, the test coverage can also be computed using the tolerance information. The failure to propagate the desired test signals or the failure to provide the desired test coverage for a module pinpoints a testability problem.

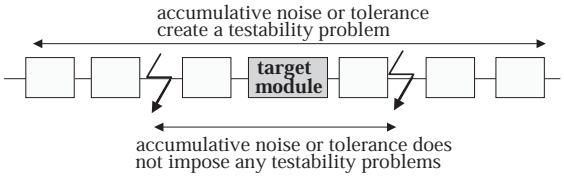
3.2 Determination of Testability Bottlenecks

With the help of the path analysis, testability problems and their causes can be determined. Since each DfT modification changes the system topology, a new analysis is needed for each solution under consideration, presumably resulting in a high number of required analyses. For example, even if only test point insertion is considered as a possible solution, there exist $(n-1)!$ distinct paths where n is the number of nodes in the system. Clearly, in order to reduce the computational complexity, a set of *promising solutions* needs to be determined using the information provided by path analysis.

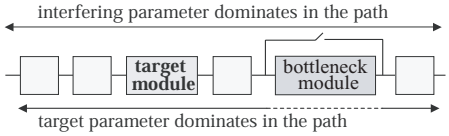
Testability problems can typically be classified into four groups, each of which requires a different approach.



a. Range deficiency problem and a representative DfT solution



b. Tolerance and noise problems and a representative DfT solution



c. Parameter interference problem and a representative DfT solution

Figure 3. Examples of viable testability solutions

Range deficiency: This problem occurs when the desired amplitude, frequency, or number of tones required for a particular test are blocked by neighboring modules. At the first level, the bottleneck is the module that most severely limits the desired signal range. A possible DfT solution to this problem needs to bypass the bottleneck module. In most cases, there may be multiple bottlenecks for one testability problem. Thus, it is essential to repeat the path analysis and bottleneck determination until the test signals are available for the target module. Figure 3a illustrates a range deficiency problem, and a viable DfT solution using an on-chip signal generator.

Noise: Noise can block controllability or observability of test signals that require small powers. In most cases, certain modules, such as mixers, contribute the highest component of cumulative noise. If the noise generated by a module singlehandedly exceeds the desired signal power, that module can be considered to be the first level bottleneck. In some cases, there may be no single module that dominates in terms of noise generation, necessitating a partitioning of the path, as shown in Figure 3b, where test point insertion is used as the DfT approach.

Parameter Tolerance: Variations in circuit parameters introduce uncertainty to the test signal attributes, thus resulting in measurement errors. While there is no simple function relating tolerance and test coverage, a probabilistic approach can be taken to compute the test coverage for each parameter to be tested [11]. Parameter tolerances can accumulate to a point where the test coverage falls below the desired levels. As in the case of noise, a specific module may be the the major contributor to the accumulated tolerance and may be marked as the bottleneck. However, in most cases, tolerances are evenly distributed among mod-

ules in the path, requiring the partitioning of the path, as shown in Figure 3b.

Parameter Interference: The parameter interference problem is typically encountered for target specifications related to non-ideal behavior, such as non-linearity or noise. For example, both an amplifier and a mixer on the same path generate third order harmonic distortion, which may need to be tested independently. While testing the IIP_3 parameter, the third order distortion component of the amplifier becomes the test signal, which will be corrupted by the distortion of the mixer. It may be argued that a detailed simulation of the mixer can be used to extract information about the power and the phase of its third order distortion component. However, even if detailed transistor level simulations are used, considering parametric variations, the extracted information typically is of no value as it contains high degrees of variation. As an example, the third order harmonic phase for a mixer may vary between $-\pi$ and π depending on the direction and the amount of component mismatch. Thus, the bottleneck module needs to be taken out of the test path when a parameter interference problem is encountered, as shown in Figure 3c, where a false path is used as the DfT solution.

The identified testability problems need to be prioritized in order to reduce the solution space. Testability problems with particular bottlenecks are more restricted in terms of the DfT choices while testability problems that suffer from cumulative noise or tolerance are more flexible. Thus it is beneficial to start with the most strict testability problems and dynamically generate solutions. In this work, testability problems are ranked with respect to the severity of the bottleneck as determined by the number of possible solutions. Problems with no distinctive bottleneck are handled last, as previously identified solutions may already have resolved these problems.

3.3 Problem Formulation

While there may be multiple testability solutions for a particular problem, each solution may provide a distinct level of test coverage and may add a certain level of overhead. Thus, it is essential to develop a methodology to select a cost-efficient set of DfT solutions such that each testability problem is solved, the cost is minimized, and the coverage is maximized. Figure 4 illustrates a graph representation of this problem, modeled as a min-cost set cover problem. This well-known graph problem is $NP-$hard, since the set-cover problem itself is $NP-$complete [13].

Since DfT approaches that do not provide the required level of test coverage for each target parameter are not included in the solution set, the primary goal in DfT selection is to minimize the overhead. Thus, we employ a two-step approach to achieve the most cost-efficient solution. First a *minimal* set of DfT solutions is selected using an optimal algorithm. The selected set constitutes the lower-bound on the overhead and is used as the intermediate solution. A simulated annealing algorithm is then utilized to increase test coverage.

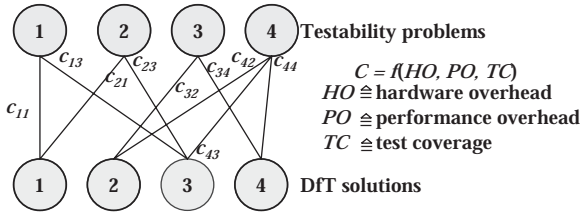


Figure 4. Graph modeling of DfT selection

3.3.1 ILP formulation to minimize DfT overhead

In order to formulate the problem for ILP, one needs to concentrate on specific testability solutions. While the proposed method can be used in conjunction with any set of DfT approaches, we use test point insertion as a representative DfT solution in this work. We formulate the problem of selecting the minimal set of test point as follows: Given p parameters, q controllability and observability pairs $\{C, O\}$, m controllability nodes, and m observability nodes, select a set of $\{C, O\}$ pairs, such that the number of controllability and observability nodes used is minimized.

Let $C_i = 1$ if controllability node i is selected, $C_i = 0$ otherwise. Let $O_i = 1$ if observability node i is selected, $O_i = 0$ otherwise. Also, let $x_i = 1$, if pair i is selected. $x_i = 0$ otherwise and $y_{ij} = 1$, if pair i can cover parameter j, $y_{ij} = 0$ otherwise. Using these variable definitions, a mathematical programming model is presented below.

Objective: Min. $J = \max_j \sum_i^m (C_i + O_i)$, subject to

1. $\forall j \sum_i^q x_i \cdot y_{ij} \geq 1$, $1 \geq j \geq p$, i.e. every parameter is covered by at least one $\{C, O\}$ pair.
2. For every controllability node k ($1 \leq k \leq m$ belonging to $\{C, O\}$ pair i ($1 \leq i \leq q$),
$x_i \cdot C_k + 1 - x_i > 0$ i.e., if pair i is chosen controllability node of that pair is also chosen.
3. For every observability node k ($1 \leq k \leq m$) belonging to $\{C, O\}$ pair i ($1 \leq i \leq q$),
$x_i \cdot O_k + 1 - x_i > 0$ i.e, if pair i is chosen observability node of that pair is also chosen.

The constraints of this mathematical programming model must now be linearized in order to express them in the form of an ILP model. The non-linear terms $x_i \cdot C_k$ and $x_i \cdot O_k$ from constraints 2 and 3 can be linearized by replacing them with variables w_{ik} and d_{ik} respectively. Now, the second constraint of the model can be re-written as follows:

(i) $w_{ik} + 1 - x_i \leq 1$.
(ii) $x_i + C_k - w_{ik} \leq 1$.
(iii) $x_i + C_k - 2 \cdot w_{ik} \geq 0$. Constraints (ii) and (iii) can be explained as follows. Consider first the case when $x_i = 0$, from (ii) and (iii) we have $w_{ik} + 1 \geq C_k$ and $2 \cdot w_{ik} \leq C_k$,

since $C_k \leq 1$, w_{ik} must equal 0. When $x_i = 1$, we have $w_{ik} \geq C_k$ and $C_k + 1 \geq 2 \cdot w_{ik}$; therefore, $w_{ik} = C_k$. Similarly, the third constraint of the model can be written as the following constraints. (iv) $d_{ik} + 1 - x_i \leq 1$.
(v) $x_i + O_k - d_{ik} \leq 1$.
(vi) $x_i + O_k - 2 \cdot d_{ik} \geq 0$.

Again, the relationship between O_k and d_{ik} is the same as the relationship between C_k and w_{ik}. We use the ILP solver called $lpsolve$ [12] to achieve a solution.

3.3.2 Cost functions

In order to extend the method to other DfT solutions, such as false paths, on-chip signal generation, or built-in-self-test, the hardware cost of each DfT overhead needs to be determined. For a particular solution, the DfT overhead can be defined in terms of hardware and performance overhead, and can easily be incorporated into the ILP formulation by changing the objective from minimization of the number of test points to minimization of the overall cost.

As explained in the previous sections, each of the identified potential DfT solutions provides the minimum required degree of test coverage. However, it is still beneficial to increase test coverage without increasing the DfT overhead. In the second phase of the algorithm, we employ a heuristic approach based on simulated annealing to increase the test coverage from the initial solution.

4 Experimental results

The proposed method is applied to a transceiver architecture where test point insertion is used as the DfT approach. While the proposed method can be used in conjunction with any DfT approach, the use of test point insertion as the sole possible solution enables a quantitative evaluation of the benefits of the proposed methodology.

The block diagram of the experimental circuit is shown in Figure 5. The dynamic range for the receive path is from -70dBm to -20dBm. In order to supply this dynamic range, a 8-bit ADC in conjunction with two variable gain amplifiers, a coarse VGA and a fine VGA, are used. The maximum output power of the transmit path is 20dBm. The in-band synthesizer phase noise is specified at -95dBc with a loop bandwidth of 300kHz, and the 8MHz-DAC spurious emissions are suppressed by a low-pass filter (LPF_1) with a bandwidth of 1MHz. The channel filter (LPF_2) bandwidth is 500kHz. The complete list of system specifications is given in the first two columns of Table 4.

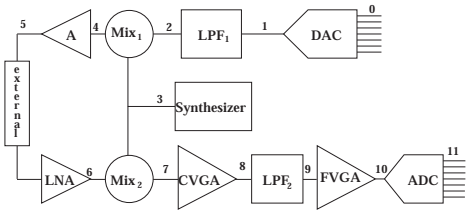


Figure 5. Experimental System

In the first step of the proposed method, an overall path analysis is conducted from the DAC to the ADC. The minimum acceptable test coverage is set at [1] 95%. Due to the aggressive test strategy, a number of testability problems prevent the use of the complete path. Specifications which can be tested through the complete path are the f_c of LPF_1, P_{1dB} of Mix_2, the gain increments of the $CVGA$ and $FVGA$, and the in-band synthesizer phase noise. The set of testability problems identified through path analysis is given in Table 4.

The testability bottlenecks can be determined by examining the cause of the testability problem. As an example, the test for the amplifier (A) bandwidth results in a range deficiency problem. The first level bottlenecks for this problem are the low-pass filters (LPF_1 and LPF_2). The complete set of testability problems and the identified first level bottlenecks are shown in Table 4. For some tests, such as the stop-band gain of the low-pass filter, it is not possible to identify a single bottleneck, since the testability problem arises from a cumulative event. Such problems are handled last since the solutions of more restrictive problems may already resolve the problems of cumulative nature. In the next phase, the DfT selection problem is formulated in terms of integer linear programming to minimize the number of test points. Table 4 also shows the selected DfT solution for each testability problem. While the use of ILP ensures minimal DfT overhead, the test coverage may be increased by a second-pass using a simulated annealing approach. In the last step of the methodology, this heuristic algorithm modifies the CO set as {(0,2,3,4,5,9), (1,2,4,5,6,11)}, increasing the test coverage for P_{1dB} and NF of Mix_1, without increasing the DfT overhead. Overall, 8 internal nodes have been selected for controllability or observability compared to 13 that would have been necessary without the proposed approach. A 39% reduction in DfT overhead is achieved with the proposed approach over path-based testing. Traditional isolated module-based testing requires C/O capabilities for all internal nodes. Thus, compared to a traditional approach, a 55% reduction can be achieved with path based testing and the proposed testability analysis methodology.

5 Conclusion

The increasing number of mixed-signal paths in today's systems necessitates innovative system-level test solutions. Path-based test development has showed promise for providing a cost-effective solution. However, in most cases, the complete signal path proves to be insufficient in providing the test access mechanism with the desired level of

[1] 5% loss in test coverage is distributed over loss in fault coverage and loss in yield coverage. [8] and [11] provide a detailed explanation of the computation of overall tolerances and test coverage.

Module	Spec	Test Prob	1st Bottl.	Possible Solutions	Selected Solutions
DAC	V_{off}	Interf.	LPF_1	{0,1}	{0,1}
	DNL	Noise		{0,1},{0,2}	{0,1}
LPF_1	G_{sb}	Noise		{0,2}, {1,2}	{1,2}
Mix_1	IIP_3	Interf.	Mix_2	{1,4}, {2,4}	{1,4}
	P_{1dB}	Range	DAC	{1,4}, {1,5}, {1,6}, {1,7}, {1,8}, {1,9}, {1,10}, {1,11}, {2,4}, {2,5}, {2,6}, {2,7}, {2,8}, {2,9}, {2,10}, {2,11}	{1,4}
	NF	Interf.	PLL	{1&3,4}, {1&3,5}, {1&3,6}, {2&3,4}, {2&3,5}, {2&3,6}	{1&3,4}
A	BW	Range	LPF_1	{2,5}, {2,6}, {2,7}, {2,8}, {4,5}, {4,6}, {4,7}, {4,8}	{4,5}
	IIP_3	Interf.	Mix_1	{4,5}, {4,6}	{4,5}
LNA	NF	Interf.	PLL	{4,6}, {5,6}	{5,6}
Mix_2	IIP_3	Interf.	Mix_1	{5,7}, {5,8}, {5,9}, {5,10}, {5,11}, {6,7}, {6,8}, {6,9}, {6,10}, {6,11}	{5,11}
	NF	Interf.	PLL	{3&4,7}, {3&4,8}, {3&4,9}, {3&4,10}, {3&4,11}, {3&5,7}, {3&5,8}, {3&5,9}, {3&5,10}, {3&5,11}, {3&6,7}, {3&6,8}, {3&6,9}, {3&6,10}, {3&6,11}	
ADC	V_{off}	Interf.	LPF_2	{9,10}, {9,11}	{9,11}
	DNL	Nosie		{7,11}, {8,11}, {9,11}, {10,11}	{9,11}
RX	G	Tol.		{5,11}	{5,11}
TX	G	Tol.		{0,5}	{0,5}

Table 1. System specifications, testability problems, 1st level bottlenecks, possible and selected test points

test coverage for all modules, due to complications, such as accumulative noise or tolerance, interference among similar parameters in the same path, and bandwidth and amplitude limitations. Therefore, it is essential to identify a cost effective set of DfT solutions that helps achieving the desired test quality. In this paper, we provide a testability analysis and DfT insertion methodology to be used in path-based test development for mixed-signal systems. Testability analysis is conduced by isolating the desired response from the undesired response and propagating appropriate information.

Testability problems are determined in terms of parameters that cannot be effectively tested and these problems are grouped under four categories. A two-step DfT selection algorithm determines the minimal set of DfT modifications and aims at increasing test coverage without sacrificing optimality for overhead. Experimental results on a transceiver path indicate a 40% reduction in the DfT overhead compared to path-based test development without a systematic DfT insertion method, and a 55% reduction in DfT overhead compared to traditional module testing.

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