An Infrastructure IP for On-Chip Clock Jitter Measurement

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Abstract

In this paper, we present an infrastructure IP core to facilitate on-chip clock jitter measurement. In the proposed approach, the clock signal under test is delayed by two different delay values and the probabilities it leads the two delayed versions are measured. The RMS period jitter value can then be derived from the probabilities and the delay difference. Both behavior and circuit simulations are performed to validate the proposed technique and analyze the design tradeoffs, and a prototype chip has been designed for further validation.

1. Introduction

In modern high-speed systems, the quality of the clock signal is crucial because most activities are synchronized to the clock. In reality, however, the clock edges may deviate from their ideal positions in the existence of jitter. To tolerate this, one has to lengthen the clock period, which degrades the system performance. The clock jitter problem gets more severe as the clock frequency multiplies because it can easily consume a large portion of the already tight timing budget. However, measuring high-speed clock jitters has been a difficult task because it usually relies on expensive ATE (automatic test equipment) and takes long test times.

One promising solution to measuring clock jitter is built-in self-test (BIST). Since on-chip BIST circuitry can be made close to the signal sources under test, accessing embedded clock signals becomes much easier and is not limited by the bandwidth of the I/O pins. The main concerns about BIST are the incurred area/performance overhead and the achievable test accuracy.

Many research efforts have been devoted to jitter testing. In [8], the authors employ a variable delay line to record the 15.9% and 84.1% points of the jitter's cumulative distribution function (CDF) curve from which the RMS jitter value can be derived. (The jitter is assumed to be Gaussian.) The main advantage is that the BIST circuit is fully digital, and thus can be more easily integrated into the design flow. The technique reported in [5] is similar to [8]; however, only two points along the CDF curve are sampled to derived the RMS jitter.

High-resolution time-to-digital techniques can also be used for jitter measurement. The techniques in [4] and [10] use a vernier delay line to achieve high-resolution jitter measurement. The limitation is the large hardware overhead and the stringent delay line linearity requirement. The technique reported in [2] intends to solve the linearity problem by using a component-invariant vernier delay line. The main limitation is the associated long test time. In [9], the authors solve the delay line linearity problem by characterizing the non-linearity and incorporating this information during the analysis phase. The VCOBIST technique [1] employs two ring oscillators to measure the time between two successive clock edges for jitter measurement.

In [12] and [11], an analytic signal method to extract peak-to-peak and RMS jitter is proposed and validated with commercial processors. The technique can reduce the test time significantly, but is not suitable for BIST applications. The method is further extended in [13]. Application of the Morlet wavelet transform to detect the phase and frequency variations of radio-frequency signals are reported in [7]. However, the technique is more suitable for ATE.

In [3], the authors propose to use the signal under test as the clock signal to an ADC which samples a sinusoidal signal. This way, the jitter information can be extracted from the ADC outputs.

In this paper, we present an infrastructure IP (IIP) to facilitate the RMS period jitter measurements of clock signals under the assumption that the period jitter is Gaussian. Compared to previous approaches, the proposed jitter measurement circuitry is quite simple—it utilizes a two-tap delay line and a phase comparator to extract and digitize the jitter information, and relies on digital resources to record the probabilities and to perform post-analysis. Since the delay line is a two-tap one, there is no linearity requirement on the variable delay line. In addition, we only need to know

the difference between instead of the actual values of the two delays, which is more feasible in a BIST environment. The main challenge is to make sure that the delay line values are within the acceptable range even in the existence of process variations. Behavior simulations are performed to analyze the non-ideal factors, and Spice simulations show promising results.

This paper is organized as follows. In section 2, we introduce the proposed technique. In Section 3, practical design issues are discussed. The circuit simulation results are shown in Section 4. Finally, we conclude this paper in Section 5.

2. The proposed technique

Assuming that the period jitter associated with the clock signal under test is a Gaussian random variable, the objective of the proposed technique is to obtain the period jitter's RMS value.

In the following discussion, for convenience, the term "jitter" will correspond to "period jitter," and below is a list of notations used throughout this paper.

$F_X(x)$**:** The normalized Gaussian CDF.

S, S'**:** S is the clock signal under test, and S' is S delayed by d_1 or d_2.

T**:** The ideal period of S.

$d_1, d_2, \Delta d$**:** d_1 and d_2 are the two delay values associated with the two-tap variable delay line, and $\Delta d = |d_1 - d_2|$.

p_1, p_2**:** p_1 and p_2 are the probabilities that S leads S' when the delay line value is d_1 and d_2, respectively.

$x_1, x_2, \Delta x$**:** $x_1 = F_X^{-1}(p_1)$, $x_2 = F_X^{-1}(p_2)$, and $\Delta x = |x_1 - x_2|$.

J, RMS_J**:** J denotes the period jitter associated with S, and RMS_J is the RMS value of J.

2.1. The basic idea

The basic idea of our approach is depicted in Fig. 1. On the left hand side of Fig. 1, A and B are two consecutive rising edges of S, and A' is the rising edge of S' corresponding to A. Since S is with Gaussian period jitter, the position of B relative to A is also a Gaussian distribution centered at T.

Now, let's consider the phase relationship between B and A'. Obviously, if S is jitter-free, the relationship between B and A' is constant and depends on d and T—B will lead/coincide with/lag A' if d is greater than/equal to/less than T. However, in the existence of jitter, the time duration between A and B, and accordingly the phase relationship (lead or lag) between B and A', will depend on the period jitter associated with that cycle and is no longer constant. In fact, the probability p that B leads A' is

$$p = F_X\left(\frac{d-T}{RMS_J}\right) \tag{1}$$

and is shown on the right hand side of Fig. 1.

At first sight, it seems that RMS_J can be derived once p and d are known, i.e.,

$$RMS_J = \frac{d-T}{F_X^{-1}(p)} \tag{2}$$

However, this intuitive approach is not suitable for BIST applications because it is difficult to measure d accurately with on-chip resources.

To avoid measuring the actual delay value, we propose to delay S by two different delays, d_1 and d_2, and measure the corresponding probabilities, p_1 and p_2, that B leads A' (Fig. 2). Rearranging Eq. 2 for d_1 and d_2, one has

$$d_1 - T = RMS_J \cdot F_X^{-1}(p_1) \tag{3}$$
$$d_2 - T = RMS_J \cdot F_X^{-1}(p_2) \tag{4}$$

From Eq. 3 and 4, RMS_J can be derived:

$$RMS_J = \frac{d_1 - d_2}{F_X^{-1}(p_1) - F_X^{-1}(p_2)} \tag{5}$$
$$= \frac{d_1 - d_2}{x_1 - x_2} \tag{6}$$
$$= \frac{\Delta d}{\Delta x} \tag{7}$$

Note that in Eq. 7, Δd, instead of d_1 and d_2, is employed to solve RMS_J. As will be shown later, this is is a more feasible solution when only on-chip resources are available.

2.2. Solving the inverse Gaussian CDF

The main difficulty of deriving RMS_J using Eq. 7 is how to solve F_X^{-1} efficiently and accurately. Clearly, solving $x_i = F_X^{-1}(p_i)$ using either F_X or the approximation function (due to Brjesson and Sundberg, 1979 [6] and with a maximum absolute error of 0.27% for any $x \geq 0$) is too computation intensive to be a practical solution. Therefore, in our approach, we propose to use a pre-computed lookup table stored on-chip or in the external ATE to realize the inverse CDF function.

2.3. The jitter measurement IIP

The proposed jitter measurement IIP is shown in Fig. 3. The jitter measurement portion the proposed IIP includes the two-tap delay line, the phase comparator, and

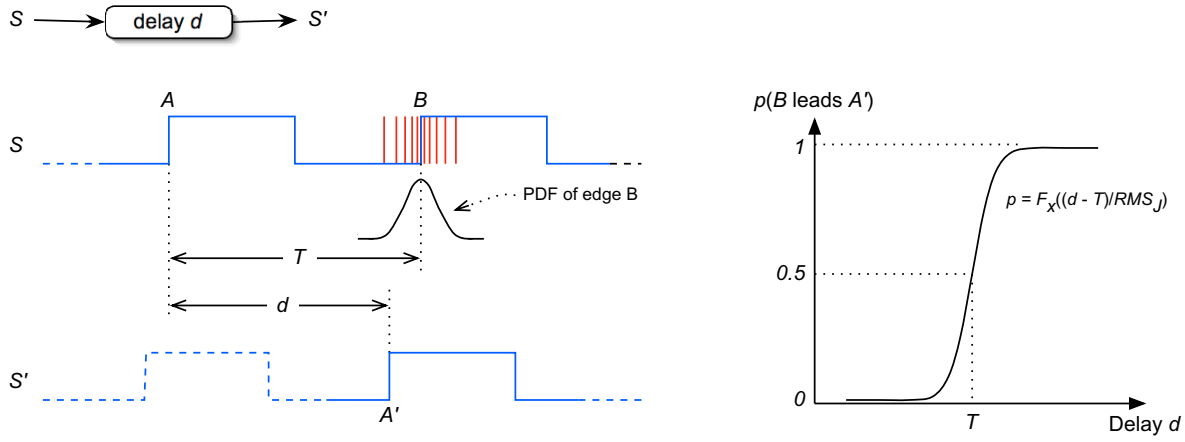

Figure 1. The basic idea.

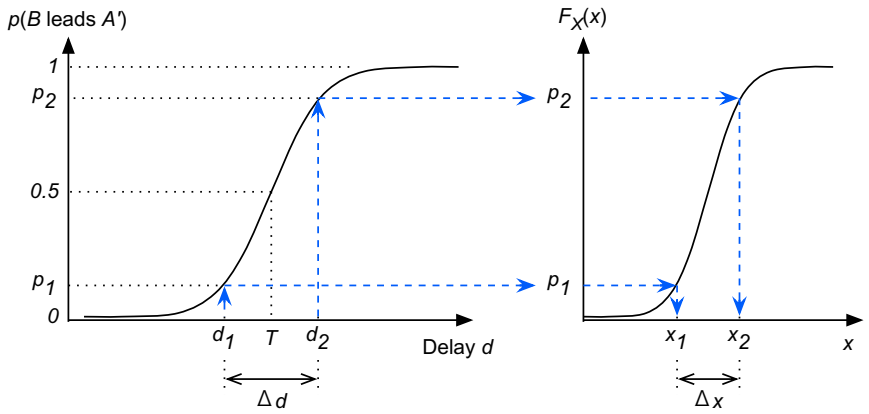

Figure 2. The proposed method.

the lead counter. The delay line is controlled by the signal $delay\_ctrl$ to generate two delay versions of clk_{test}, the clock under test. The phase comparator, on the other hand, determines whether the rising edge of S leads or lags that of S'. The lead counter keeps track of the number of times S leads S'.

The inverter, switches, and the frequency counter forms the calibration portion of the IIP to measure Δd. Note that clk_{ref} is a reference clock for frequency counting.

2.4. The measurement procedure

The jitter measurement procedure consists of three phases: calibration, measurement, and analysis.

In the calibration mode, ϕ_m is low and ϕ_c is high. This way, the inverter together with the delay line forms an oscillator. Let the inverter delay be d_{inv}. The $delay\_ctrl$ signal is set to low and high to measure $(d_1 + d_{inv})$ and $(d_2 + d_{inv})$, respectively.

In the measurement mode, ϕ_m is high and ϕ_c is low. N phase comparisons between S and S' are performed for both delay values, and the number of times S leads S', denoted by n_1 and n_2 respectively, are counted and stored for later analysis.

Finally, in the analysis phase, Δd, p_1, and p_2 are first derived:

$$\begin{aligned} \Delta d &= (d_1 + d_{inv}) - (d_2 + d_{inv}) \\ p_i &= \frac{n_i}{N} \end{aligned}$$

x_1 and x_2 are then derived using the pre-computed inverse CDF table. RMS_J is then computed using Eq. 7.

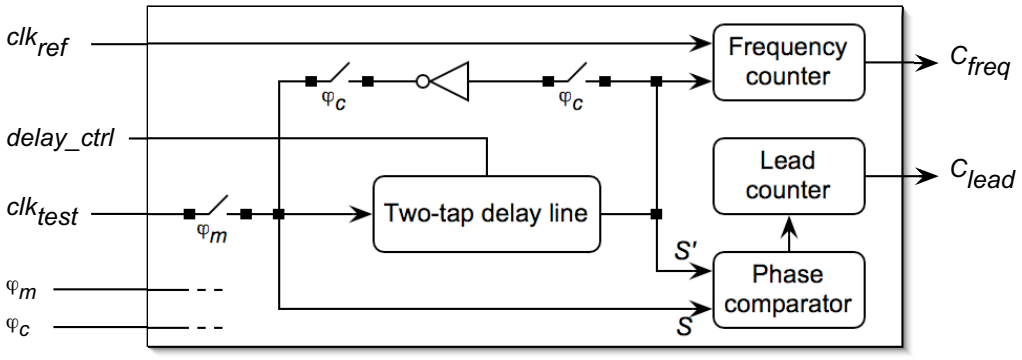

Figure 3. The proposed jitter measurement infrastructure IP.

3. Error analysis and simulation

In this section, we will analyze and discuss the impacts of the non-ideal factors on the IIP design.

3.1. The finite sample size

Ideally, the number of phase comparisons, N, should be as large as possible so that the sample distribution is close enough to the theoretical one. In reality, N is nevertheless limited by the available test time, which causes the sampled CDF to deviate from the ideal one. In our method, this deviation results in errors in p_i's, and eventually in x_i's. The incurred error can be reduced by using the largest possible N.

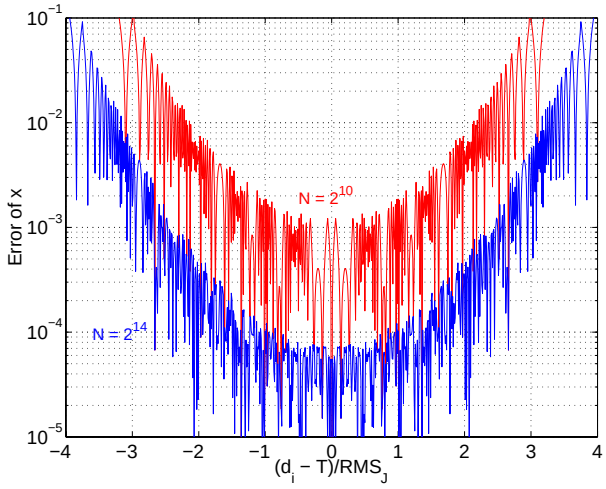

Figure 4. Quantization error.

Another effect of the finite N on p_i's is the quantization error. As $p_i = n_i/N, 0 \leq n_i \leq N$, p_i can assume only the $N+1$ discrete values, i.e., $\left\{\frac{0}{N}, \frac{1}{N}, \frac{2}{N}, \cdots, 1\right\}$; thus, the quantization error associated with the measured p_i's is bounded by $\frac{1}{N}$. The errors of p_i's are later translated to errors in x_i's. In Fig. 4, the x-axis is $(d_i - T)/RMS_J$, the y-axis is the resulting error in x_i, and the upper and lower curves correspond to $N = 2^{10}$ and $N = 2^{14}$,

respectively. The bathtub-like curves are due to the very steep tails in both directions of the inverse Gaussian CDF function, and suggest that $|d_i - T|$ should be within a few RMS_J's of T so that the errors of x_i's are acceptable. Take $N = 2^{10}$ for example, if d_i's are selected such that

$$|d_i - T| \leq 2 \cdot RMS_J \tag{8}$$

then the induced error in Δx will be bounded by 2%. Clearly, the errors can be effectively reduced by increasing N. Note that as Δx is the divider of Eq. 7, while making d_i's closer to T reduces the quantization error, d_i's should be kept far enough so that the resulting Δx is sufficiently large.

3.2. The measurement error of Δd

From Eq. 7, the error of RMS_J is proportional to that of Δd. Thus, one should increase the frequency counting duration to enhance the accuracy.

3.3. Behavior simulation

For convenience, we define window_center $= \frac{d_1+d_2}{2}$ and window_size $= |d_1 - d_2|$.

A behavior model of the proposed BIST circuitry is constructed to evaluate the effect of the limited sample size, and the measurement results for $N = 2^{10}$ are shown in Fig. 5. In Fig. 5, the x and y axes correspond to $(\text{window\_center} - T)/RMS_J$ and $\text{window\_size}/RMS_J$ respectively, and the z axis is the measurement results normalized by RMS_J. For ease of visualization, results greater than 1.2 or less than 0.8 are clipped. Fig. 5

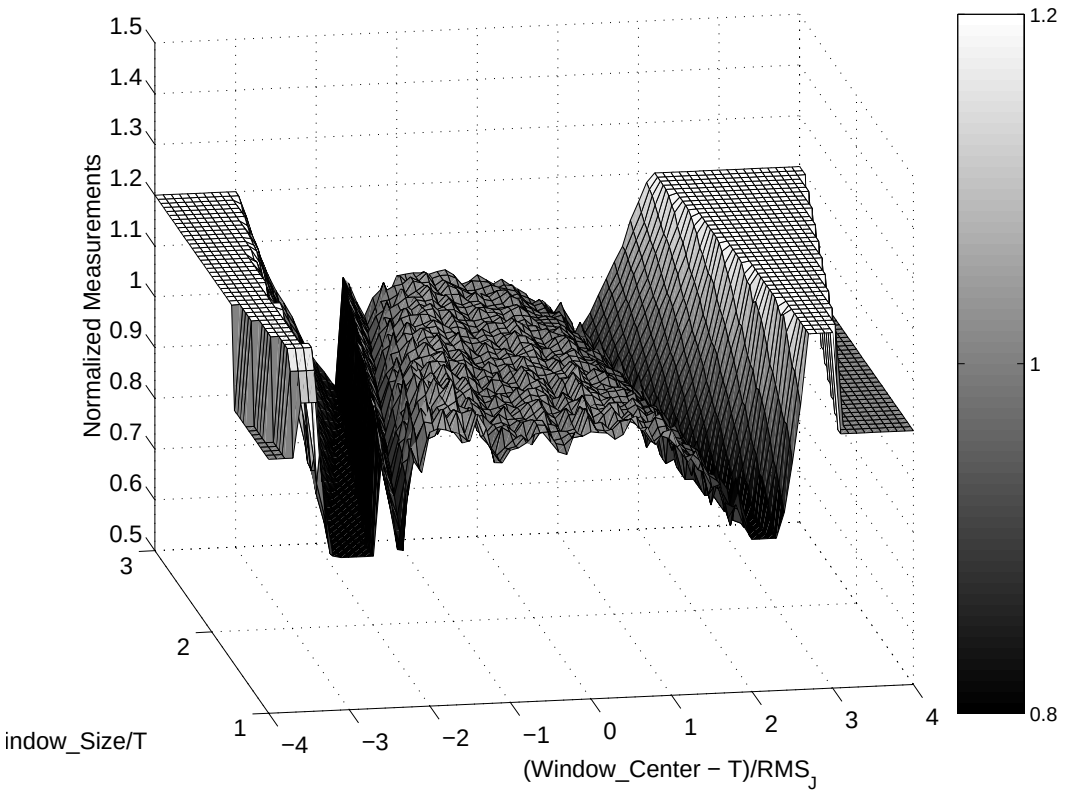

Figure 5. Behavior simulation for $N = 2^{10}$.

shows that the measurement result is more stable and accurate when the window center is around T, and the measurement errors increase dramatically after the window center moves outside the stable region. Note that the width of the stable region decreases with growing window size.

To determine the design values of d_i's, we set the acceptable measurement error to be $0.05 \cdot RMS_J$. (In practice, the threshold is determined by the designer or the test engineer according to the applications and test requirements.) Not shown here, the acceptable combinations of window center and size forms approximately a trapezoid symmetric about window_center = T. Also, the pass region becomes narrower as the window size multiplies because one or both d_i's are pushed toward the steep tails of the inverse Gaussian CDF curve where the error caused by the limited sample size is considerably amplified.

Thus, to make the IIP more immune from process variations, the center of the pass region is selected as the delay-line design target, which corresponds to

$$d_1 = T + RMS_J \quad (9)$$
$$d_2 = T - RMS_J \quad (10)$$

Eq. 9 and 10 may look odd because they both contain the term RMS_J that is to be measured! In practice, one can substitute RMS_J in the two equations with the specified pass/fail threshold. For example, for a 1 GHz signal, if the pass/fail threshold is 40 ps, the delay line should be designed to have delay values of 960 and 1,040 ps.

4. Simulation results

To validate the proposed technique, Spice simulations are performed with the following setup: (1) T = 1 ns, (2) the jitter pass/fail threshold is 40 ps, and (3) $N = 1,000$. Based on the specifications, the delay line is designed to have delay values $(d_1, d_2) = (960, 1040)$ ps.

In the calibration mode, the measurement results are $(d_1 + d_{inv}) = 1,152$ ps and $(d_2 + d_{inv}) = 1,230$ ps. Thus, we have Δd = 78.7 ps which is quite close to the design target of 80 ps.

The simulation results for different RMS jitter values are shown in Table 1. In Table 1, the first column lists the injected RMS jitter values, the second and third columns are n_1 and n_2 respectively, the fourth column is $\Delta x = (x_1 - x_2)$, and the last two columns are the absolute and

RMS jitter (ps)	n_1	n_2	Δx	Result (ps)	Error	
					ps	%
30	99	866	2.395	32.8	2.8	9.5
40	154	813	1.9084	41.2	1.2	3.1
50	204	775	1.5828	49.7	0.2	0.5
60	239	712	1.2688	62.0	2.0	3.3
70	293	684	1.0237	76.8	6.8	9.8

Table 1. Simulation Results

relative errors. From the n_1 and n_2 values, we can see that d_1 and d_2 are not symmetric about 1,000 ps. The RMS jitter measurement errors are within 5% for 40–60 ps RMS jitter; however, the errors grow as the difference between RMS_J and the pass/fail threshold increases.

The simulation results in Table 1 show that the measurement errors of this technique grows with increasing difference between RMS_J and the pass/fail threshold, which seems to be a limitation. Indeed, this makes the proposed technique less suitable for characterization testing. However, the technique can work well in pass/fail testing because the accurate measurement around the test specification reduces the chance of mis-classifying devices close to the specification. On the other hand, for devices well above or below the test specification, the measurement error is still small enough so that they won't be mis-classified, either.

Deviations of d_1 and d_2 from their desired values due to process and/or temperature variations can also lead to test inaccuracies. To solve this problem, we may modify the variable delay so that it has more than two different delay values. This way, if only two of the delay values are close to the desired values, the test accuracy can be ensured.

5. Conclusion

In this paper, we present an RMS period jitter measurement technique intended for BIST applications. By comparing the phases of the clock signal under test and two of its delayed versions, information about the jitter's CDF curve is extracted and RMS jitter can thus be derived. Since only two points on the CDF curve are needed, the test circuitry is quite simple. Behavior simulations have been performed to analyze the limitation of the proposed technique. We have designed a prototype chip for fabrication. In the future, we will develop a fully digital implementation of the proposed technique to further reduce the circuit complexity.

Acknowledgment.

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