An Architectural Power Estimator for Analog-to-Digital Converters

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Abstract

This paper presents an architectural power estimation tool that can accurately estimate the power consumptions of analog-to-digital converters. Combining the advantages of both the bottom-up approach and the top-down approach, the estimator can help AMS SoC designer on high level power optimized design without detailed knowledge of the circuit. The three-stage estimation process makes the estimator appropriate for architectural exploration of designs employing low power techniques. The framework makes it convenient to evaluate power dissipation of new customized architectures. Experimental results for 19 commercial designs show good estimation accuracy.

1. Introduction

To achieve the power optimized design goal for the mixed-signal SoC, attention must be paid to minimize the power consumption at the beginning of system design. On the other hand, system level designers often have little knowledge about the detailed circuit techniques, making it hard to evaluate the performance-power trade-off at high level. To tackle this problem, the development of high level mixed-signal component models and power estimators to be used in system-level design tools is necessary for effective performance-power tradeoffs.

Compared with intensive research on various digital building blocks, work on power modeling and estimation for analog/mixed-signal (AMS) building blocks is relatively insufficient. This basically comes from the fact that the architectures of AMS circuits, when designed, are less regular compared with their digital counterparts, making it harder to model their power performance.

Used as the interface of analog and digital portion, Analog-to-Digital Converter (ADC) is the key function unit of a mixed-signal system and must be optimally designed considering both performance and power. Lauwers and Gielen proposed power modeling and estimation for ADC using equation-based models [1]. A numerical power consumption value is calculated as a function of ADC performance parameters. The power model is derived from fitting parameters, which means the estimated results can only represent the average number for a given ADC specification. Therefore, it is often difficult to achieve high accuracy when specific low-power techniques are applied to one or more of the ADC components. Its result contains almost no topology information, thus contribute little to the low-level circuit designers in next stage of the design hierarchy.

The power estimator proposed in this paper combines the advantages of both the bottom-up approach and the top-down approach. System-level designer can easily use the tool without detailed knowledge of circuit topology. The tool can also provide the topology information that best suites the performance requirement and it can achieve very good accuracy of power estimation. The information can be used to guide the detailed design of ADC components.

2. Power estimator for ADC

2.1. Power estimation framework for ADC

The framework of power estimation for ADC is shown in Figure 1. There are three major steps for the estimation process.

In the first step, typical ADCs are partitioned into major building block. These blocks are further divided into basic components. The major components are Comparator, Sample-and-Hold, Sub-DAC, Integrator and Gain-stage. The power consumption characteristic of these components is modeled. These component models are building blocks for the bottom up power estimation of assembled ADC. Each component may be of different types and technologies. The user specifies the technology, sampling rate and precision. New low power technology can be modeled by adding new types and its related power model into the framework.

Then in the second step, the ADCs are categorized into different architectures and topologies. They are flash, pipelined, SAR and Sigma-Delta. Each category has its proper application in terms of sampling rate and precision.

The user can also specify a particular topology of interest. An ADC is the assembly of the basic components. The quantitative relationship between numbers of components for each category for a given precision is modeled in this step.

The third step is the synthesis. The user can specify additional requirements. An ADC is synthesized by the estimator according to the requirements. The overall power consumption is the summation of the components' power consumption. Different topologies are evaluated and the one with the lowest power consumption are reported as a result.

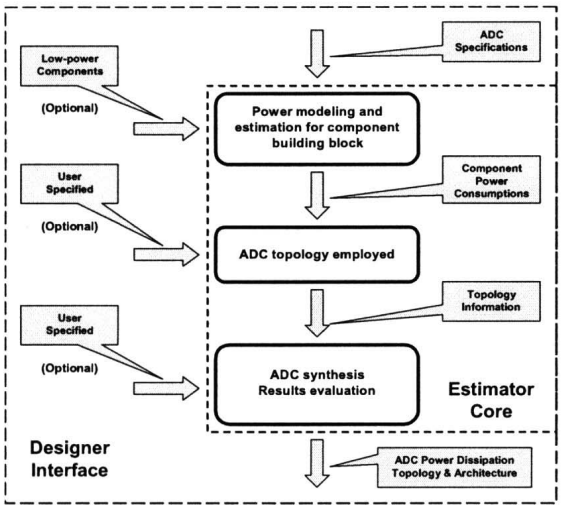

Figure 1. Framework of power estimator for ADC

2.2. Power modeling of ADC components

There are five major component building blocks for ADCs: Comparator, Sample-and-Hold, Sub-DAC, Integrator and Gain-stage. Instead of using five totally different functions to model their power consumptions, a universal function with different parameters is employed in the estimator. The advantage of doing this is that the closed form of the power modeling function provides great potential to be extended towards other (or new) building blocks. Also, the simplicity of model makes it very easy to be integrated with other system exploration tools to perform fast estimation and evaluation.

To derive the power modeling function, it is instructive to investigate some basic relationship between metrics of analog circuits. The important parameters involved are operating frequency, equivalent resistance/capacitance, effective voltage, bias current, supply voltage and power consumption. Assumptions are made in order to simplify the deduction.

In order to guarantee the speed performance, the circuits' response time constant must be small enough so that the current can charge the load capacitor to a certain voltage level that can be recognized by the following processing units. In other words, the sampling frequency is limited by the effective capacitance and load resistance of the AMS building block.

$$f_{sample} \propto \frac{1}{\tau_{eff}} = \frac{1}{R_{load} \cdot C_{eff}}$$

In most cases, the voltage gain of an AMS building block can be written as the product of its transconductance and the load resistance. For CMOS implementation, the equivalent transconductance of the circuits is proportional to g_m of the transistors, and assume the tranconductance factor k

$$A_v = R_{load} \cdot G_m = R_{load} \cdot k \cdot g_m$$

$$f_{sample} \propto \frac{1}{R_{load} \cdot C_{eff}} = \frac{k}{A_v} \cdot \frac{g_m}{C_{eff}}$$

Assume most of the transistors operate in their saturation region.

$$I_{bias} = I_{DS} = \frac{1}{2} \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot V_{eff}^{\ 2}, \text{ and } V_{eff} = V_{GS} - V_{TH}$$

$$g_m = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot V_{eff} = \frac{2 \cdot I_{bias}}{V_{eff}}$$

$$f_{sample} \propto \frac{k}{A_v} \cdot \frac{g_m}{C_{eff}} = \frac{k}{A_v} \cdot \frac{2 \cdot I_{bias}}{V_{eff} \cdot C_{eff}}$$

Rearrange the equation, and notice that the power consumption of the AMS building block equals to the product of the total bias current and the supply voltage. For long channel devices, the effective capacitance is mainly due to the gate-bulk capacitance which scales with the feature size of the process technology.

$$I_{bias} \propto \frac{1}{2} \cdot \frac{A_v}{k} \cdot V_{eff} \cdot C_{eff} \cdot f_{sample}$$

$$P = \sum I_{bias} \cdot V_{DD}, \qquad C_{eff} \propto L_{\min}$$

$$P \propto \sum \frac{1}{2} \cdot \frac{A_v}{k} \cdot V_{eff} \cdot L_{\min} \cdot f_{ssmple} \cdot V_{DD}$$

For a given AMS building block, the voltage gain A_v and the transconductance coefficient k are determined values and only depend on the circuit's structure. Therefore, the power efficiency parameter η is introduced to represent this characteristic and the equation can be written as:

$$P = \frac{1}{\eta} \cdot V_{eff} \cdot V_{DD} \cdot L_{\min} \cdot f_{sample}$$

$$\eta \propto \sum 2 \cdot \frac{k}{A_v}$$

The effective voltage of the circuits is determined by the rail-to-rail voltage range and the signal voltage swing. In order to ensure the MOS transistors work in saturation region, the sum of the maximum signal voltage swing and the effective voltage can not exceed the value of supply voltage V_{DD}. This relationship can be expressed as:

$$V_{eff} = \alpha \cdot V_{DD} - \beta \cdot V_{swing}$$

Where α and β are coefficients whose values depends on the cascode level of the building block.

In summery, the power modeling function is derived as: $$P_i = \frac{\alpha_i \cdot V_{DD} - \beta_i \cdot V_{swing}}{\eta_i} \cdot V_{DD} \cdot L_{\min} \cdot f_{sample}$$

This function has a similar format to the well-known power model for digital CMOS circuits: $P = V_{DD}^2 \cdot C \cdot f$. The value of coefficients η_i , α_i and β_i varies for different building block - Comparator, Sample-and-Hold, Sub-DAC etc, and can be derived by either experimental data fitting or low-level simulation.

2.3. Topology employed

Listed in Table 1, the estimator can optimally recommend an ADC topology type based on the performance requirement. The designer can specify a particular topology type in cases that a certain type of ADC has been determined or customized architectures will be employed in the design.

TOPOLOGY	RESOLUTION	SPEED
Flash	< 8 *bit*	> 100 *MHz*
Pipelined	9 – 14 *bit*	1 – 100 *MHz*
SAR	> 14 *bit*	> 1 *MHz*
Sigma-Delta	> 16 *bit*	> 1 *MHz*

2.4. Architectural exploration

Once a certain ADC topology has been determined and the power number of each component building block has been obtained, the estimator will generate architectural parameters and then calculate the total power consumption of the ADC through different equations.

- Flash

The architecture of a flash A/D converter is quite simple to understand. A flash A/D converter with *n -bit* resolution compares an input voltage to a large number of reference voltages set by a resistor network through $2^n - 1$ comparators connected in parallel. The outputs of comparators are then sent to the encoder. The final output of the A/D converter is determined by which two, of the $2^n - 1$ reference voltages, the value of input signal is between.

Major components: Comparator (P_{cmp}), Encoder (P_x)

Parameters: Resolution (b)

Estimation equation: $P_{flash} = (2^b - 1)P_{cmp} + P_x$

- Pipelined

Pipelined ADCs distributed the conversion process over multiple stages in sequence. Each stage but the last one consists of four basic building blocks: sample and hold, sub-ADC, sub-DAC and gain stage. The last stage only has a S/H and a sub-ADC. The analog input is applied to the first stage in the chain, and N_1 bits are detected. The analog residue is also generated and applied to the next stage. The same procedure repeats up to the end of the chain and the last stage gives the least significant N_2 bits. This concept is similar to the idea of an assembly line because the interstage sample and hold allows all of the stages to operate concurrently.

Major components: Sample-and-Hold ($P_{S/H}$),
Sub-DAC (P_{DAC}), Comparator (P_{cmp}),
Gain-Stage (P_{gain}), DEC (P_x)

Parameters: Resolution (b), Number of stage (N_{sta})

Estimation equation:

$$P_{pipe} = N_{sta}(P_{S/H} + (P_{DAC} + P_{gain})b/N_{sta} + (2^{b/N_{sta}} - 1)P_{cmp}) + P_x$$

- SAR

The A/D technique based on a successive-approximation register can provide the lowest hardware cost. The analog input voltage is held on a sample/hold. In every cycle, the reference voltage is adjusted by the control logic to implement the binary search algorithm. The comparison sequence continues all the way down to the LSB and the N-bit digital output is stored in the register.

Major components: Comparator (P_{cmp}), Sub-DAC (P_{DAC}),
Sample-and-Hold ($P_{S/H}$),
Control Logic/Register (P_x)

Parameters: Resolution: (b), Bit/cycle (m)

Estimation equation:

$$P_{SAR} = \frac{b}{m}(P_{S/H} + mP_{DAC} + (2^m - 1)P_{cmp}) + P_x$$

- Sigma-Delta

Sigma-Delta ADCs have a relatively unique conversion technique, called oversampling. They can achieve ultra high resolution by operating the circuits on a sampling frequency much higher than the data rate. The input signal passes through the integrator which feeds a comparator. The comparator output is fedback to the input summing junction via a one-bit sub-DAC. This output also passes through the decimation filter at the output of the converter. The feedback loop forces the average of the output signal to be equal to the input value.

Major components: Comparator (P_{cmp}), Integrator (P_{intg})
Sub-DAC (P_{DAC}), Gain-Stage (P_{gain})
Decimation circuits (P_x)

Parameters: Resolution (b), Number of order (N_{order}),
Oversampling rate ($R_{oversample}$)

Estimation equation:

$$P_{SD} = R_{ovsample}(N_{order}P_{intg} + P_{cmp} + P_{DAC}) + P_x$$

3. Results

By low-level simulation in Cadence SpectraS, the value of coefficients η_i, α_i and β_i in the power modeling function for different building block is summarized in Table 2.

Table 2. Coefficients in power modeling function

	α_i	β_i	$\eta_i\ (\Omega \cdot m/s)$
S/H	0.5	0.25	14.6×10^3
Comparator	0.5	0.30	32.1×10^3
Sub-DAC	0.5	0.20	27.5×10^3
Gain	0.5	0.20	28.7×10^3
Integrator	0.5	0.15	9.8×10^3

No to lose generality, 19 samples of commercial devices from several venders [2][3][4][5][6] are used to validate the power estimator. Among these samples, 3 are flash, 7 are pipelined, 5 are SAR and 4 are sigma-delta. Their resolution ranges from 6-bit to 24-bit, speed ranges from 480S/s to 800MS/s. The comparison of the estimated power consumption and the power consumption from data sheets is shown in Figure 2. The average absolute error and average relative error for each ADC topology is shown in Figure 3. The relative error is calculated as:

$$E_{relative} = \frac{\left|P_{data\_sheet} - P_{estimaed}\right|}{P_{data\_sheet}}$$

From the results, it can be seen that relative errors are around or below 20% for all the four topologies. The estimation error is relatively large for flash (20.2%) since most of commercial devices are not full-flash type, but two-step conversion or half-flash. Therefore, their actual power numbers are less than estimated results. On the other hand, the actual power numbers for SAR are larger than their estimated results (15.8%) due to the big portion of power consumed by control logic and registers in this type of ADCs. The overall relative error is 11.3%.

4. Conclusions

The architectural power estimation tool with good accuracy for analog-to-digital converts is presented, which combines the advantages of both the bottom-up approach and the top-down approach. System-level designers can use the tool without detailed circuit parameters and it can provide topology information that benefits the following detailed design process as well. The estimator also has the ability to be applied to specific low-power designs and can be easily extended to new customized designs. Based on 19 commercial devices for validation, the estimator achieves overall relative error of 11.3%.

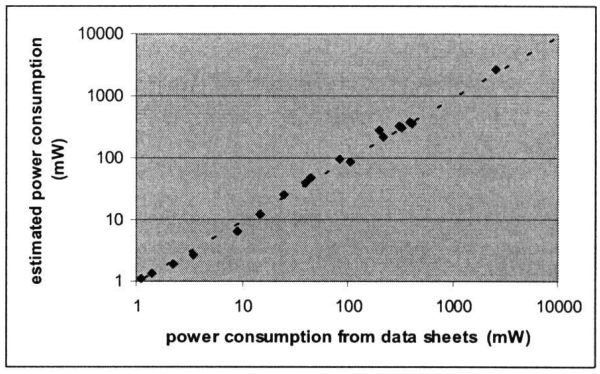

Figure 2. Comparison of the estimated power consumption and the specifications from data sheets

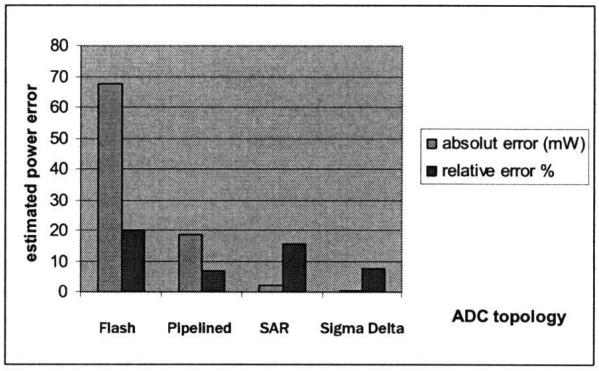

Figure 3. The average absolute error and average relative error for each ADC topology

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