A Highly-Guided *X*-Filling Method for Effective Low-Capture-Power Scan Test Generation

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***Abstract*—X-filling is preferred for low-capture-power scan test generation, since it reduces IR-drop-induced yield loss without the need of any circuit modification. However, the effectiveness of previous *X*-filling methods suffers from lack of guidance in selecting targets and values for *X*-filling. This paper addresses this problem with a highly-guided *X*-filling method based on two novel concepts: (1) *X*-score for *X*-filling target selection and (2) probabilistic weighted capture transition count for *X*-filling value selection. Experimental results show the superiority of the new *X*-filling method for capture power reduction.**

***Index Terms*—Scan test, test generation, *X*-filling, capture.**

I. Introduction

SCAN testing is the most widely adopted test scheme for logic integrated circuits. It is based on full-scan design for improving controllability and observability, automatic test pattern generation (ATPG) for test stimulus creation, and automatic test equipment (ATE) for test application. Its advantages include easy implementation, low circuit impact, strong diagnosis support, and mature tool availability [1].

However, the deep submicron (DSM) era has brought in many new challenges to scan testing, among which *test power dissipation* is a major one [2]. This is because scan test power could be twice as high as functional power, especially for large-scale, high-density, and low-power chips [3]. This excessive test power problem is rapidly becoming a major cost factor and significant yield killer [4].

As illustrated in Fig. 1, there are two types of scan test power, *shift power* and *capture power*, corresponding to the two basic scan test operations, *shift operation* and *capture operation*, respectively. New test stimuli (*A* in Fig. 1) are loaded serially in the shift operation, while internal test responses (*B* in Fig. 1) are loaded into scan flip-flops (FFs) in parallel in the capture operation.

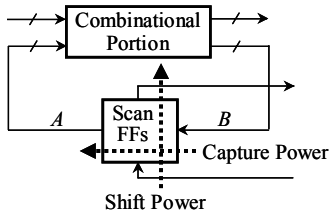

Fig. 1. Two types of scan test power.

Both shift and capture power dissipation may have *instantaneous* impact. This is because high switching activity at circuit nodes due to the non-functional characteristic of test stimuli and test responses in scan testing may cause excessive IR-drop. Consequently, flip-flop malfunctions and/or timing violations may occur, resulting in significant test-related yield loss [5, 6].

Shift power dissipation may also have *accumulative* impact. This is because high switching activity often lasts for an extended period of time due to a large number of consecutive clock pulses in the shift operation. Intensive energy consumption leads to excessive heat dissipation, which may permanently damage a chip or significantly reduce its reliability due to accelerated electromigration [7].

Instantaneous and accumulative impacts of scan test power are rapidly getting worse for large-scale, high-density, and low-power chips [3]. Therefore, it is necessary to address the test power problem in order to maintain the usefulness of scan testing. Although one can over-design the package and the power grid to accommodate high test power, this *passive* approach not only compromises the competitive edge of a design but also incurs prohibitively high costs. Therefore, the *active* approach, i.e. reducing test power itself, is more practical and desirable [2].

Shift power reduction has been intensively researched and many effective solutions are now available. Since the shift operation only needs to guarantee that scan chains operate correctly and has nothing to do with ATPG, a wide range of techniques can be fully explored to efficiently reduce shift power. Typical approaches to shift power reduction include test scheduling [8], test stimulus manipulation [9-15], circuit

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modification [16, 17], scan chain modification [18-20], and clocking scheme manipulation [5].

Although not a cause for heat dissipation, capture power is nonetheless responsible for test-induced yield loss. In a real case, a 3M-gate industrial circuit passed functional testing but failed even slow-speed scan testing. The circuit passed all scan chain flush tests but showed unstable behaviors in captured test responses. This indicated a capture problem, which was caused by the test clocking scheme that used only one test clock for all clock domains. As a rescue, one-hot clocking was brought in to reduce the number of simultaneously-operating FFs in the capture operation.

However, although test clocking schemes such as one-hot and multi-capture are capture-power-frugal, they increase test time, test data volume, and memory usage in ATPG. This often makes it difficult to apply them for a circuit with many large clock domains. Therefore, there is a need for more sophisticated solutions for capture power reduction.

Capture power reduction [11, 21-24] is more difficult than shift power reduction. This is because the capture operation is directly related to such critical issues as circuit timing and ATPG complexity, which, if not properly handled, could render a solution for capture power reduction impractical. For this reason, *X-filling* is widely considered a preferred approach to capture power reduction, as it needs no modification to circuit design or ATPG.

X-filling is the process of assigning logic values to the unspecified bits (*X-bits*) in a *test cube* so as to obtain a fully-specified *test vector* with a certain characteristic. For example, random *X*-filling has long been used in dynamic compaction for detecting more faults by a test vector [1]. Recently, a few *X*-filling methods have been proposed for capture power reduction [11, 21, 22], and they can be collectively called *LCP* (Low-Capture-Power) *X*-filling.

In addition to no circuit/ATPG impact, one more important advantage of LCP *X*-filling is its compatibility with any shift power reduction solution that is not based on the use of *X*-bits. As a result, total (shift and capture) test power reduction can be achieved. Fig. 2 shows an example of using MD-SCAN (multi-duty scan) [5] for shift power reduction and LCP *X*-filling for capture power reduction.

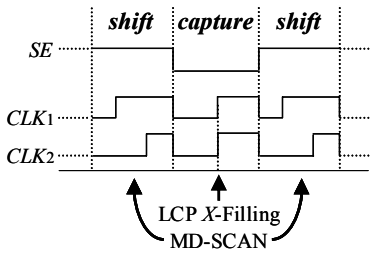


Fig. 2. A complete solution for test power reduction.

MD-SCAN lowers shift power by using multiple shift clock phases to reduce the number of simultaneously-operating FFs. It cannot reduce capture power, however, since only one capture clock phase is used in order to contain ATPG complexity and memory usage. Nonetheless, since MD-SCAN does not rely on *X*-bits, LCP *X*-filling can use the *X*-bits to generate test vectors with low capture power. This leads to a complete solution for test power reduction.

In many cases, capture power reduction is more critical than shift power reduction [24]. For example, in the case shown in Fig. 2, shift power can be readily reduced to $1/n$ if n shift clock phases are used. However, if capture power is not sufficiently reduced, the goal of total test power reduction cannot be achieved. Therefore, it is highly critical to make capture power reduction as effective as possible.

However, the effectiveness of previous LCP *X*-filling methods is far from being satisfactory. The major reason is that they suffer from the problems of lack of guidance in two key operations in *X*-filling, as described bellow:

- ***X*-Filling Target Selection Problem**: A test cube often has multiple *X*-bits, and different *X*-filling orders for the *X*-bits lead to different results in capture power reduction. However, previous LCP *X*-filling methods provide no sufficient guidance for *X*-filling target selection, which adversely affects the result of capture power reduction.
- ***X*-Filling Value Selection Problem**: After the target *X*-bit for the current *X*-filling run is selected, a proper logic value (0 or 1) should be selected for the target *X*-bit in order to reduce capture power as much as possible. However, some LCP *X*-filling methods [11,12] only try to reduce logic value transitions inside the resulting test vector by using such techniques as 0-filling, 1-filling, and minimum-transition-filling, without considering the impact of these techniques on capture power. Other LCP *X*-filling methods [21,22] only try to reduce the number of logic value transitions at the outputs of scan FFs, which does not necessarily have a good correlation with the total capture power of the whole circuit (gates and FFs). This lack of guidance in *X*-filling value selection also adversely affects the result of capture power reduction.

This paper addresses the two selection problems with a *highly-guided X*-filling method, which is based on the following two novel and powerful concepts:

- ***X*-Score**: This concept is used to quantify the impact of each *X*-bit in a test cube on capture power reduction. Structural information of a circuit, logic values of specified bits, and inter-relations among different *X*-bits, are all explored in *X*-score calculation. This makes it possible for *X*-scores to be used as quantitative guidance in selecting a proper *X*-filling target in each *X*-filling run.
- **Probabilistic Weighted Capture Transition Count**: This new metric is used to estimate the capture power of a test cube with *X*-bits by the probabilistically-estimated number of weighted capture transitions at all nodes (gates and FFs). It overcomes the limitation of the *weighted switching activity* metric [2] that can only be applied for a test vector without any *X*-bit, and significantly improves the accuracy of capture power estimation over previous methods [21,22] for a test cube. As a result, this new metric can provide better guidance in selecting a proper logic value for the target *X*-bit in each *X*-filling run.

Experimental results clearly demonstrate the advantage of using the above two sophisticated guidance techniques in LCP *X*-filling for capture power reduction.

The rest of the paper is organized as follows: Section 2 describes the background. Section 3 presents the general overview of the new LCP *X*-filling method, while Sections 4 and 5 describe *X*-filling target selection and *X*-filling value selection, respectively. Section 6 shows experimental results, and Section 7 concludes the paper.

II. BACKGROUND

A. X-Filling for Capture Power Reduction

A *test cube* is a partially-specified input bit combination with at least one don't-care bit, while a *test vector* is a fully-specified input bit combination without any don't-care bits. A don't-care bit is also called an *X-bit*.

Test cubes can be generated during ATPG. *X*-bits usually exist in a test cube since not all input bits need to be specified in order to detect one or more target faults. Test cubes can also be obtained from test vectors by *X*-bit identification methods [25]. Generally, a large portion of bits in a set of fully-specified test vectors, as much as over 60% in many cases, can be turned into *X*-bits without incurring any fault coverage loss.

In this paper, LCP *X*-filling is conducted for the *X*-bits in a test cube for the purpose of reducing the capture power of the resulting test vector. As illustrated in Fig. 3, *c* is a test cube with three *X*-bits, and the result of *X*-filling *c* is a test vector *v* with no *X*-bit.

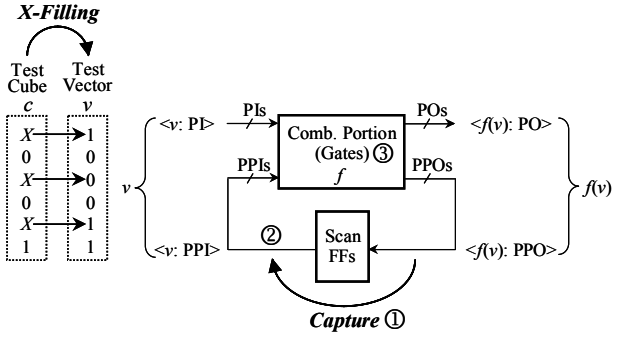


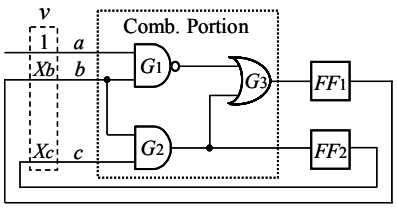
Fig. 3. LCP *X*-filling and its effect.

In Fig. 3, *v* has a primary input (PI) part and a pseudo primary input (PPI) part, denoted by <*v*: PI> and <*v*: PPI>, respectively. <*v*: PI> is applied directly and <*v*: PPI> is applied through scan shift. The test response of the combinational portion is *f*(*v*), which has a primary output part and a pseudo primary output part, denoted by <*f*(*v*): PO> and <*f*(*v*): PPO>, respectively. The capture operation (①) is to load <*f*(*v*): PPO> into scan FFs to replace <*v*: PPI>. If <*v*: PPI> ≠ <*f*(*v*): PPO>, *FF transitions* (②) will occur at the outputs of some scan FFs, which will lead to some *gate transitions* (③) in the combinational portion. FF transitions and gate transitions, collectively called *capture transitions*, result in capture power dissipation.

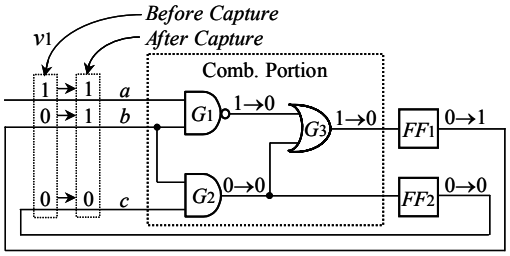
From Fig. 3, it is clear that LCP *X*-filling has two key operations: *X-filling target selection* and *X-filling value selection*. That is, if a test cube has multiple *X*-bits, it is necessary to select one *X*-bit as the target *X*-bit for each *X*-filling run. Then, a proper logic value needs to be selected for the target *X*-bit. These two operations are repeated until there is no more *X*-bit. Obviously, sufficient guidance should be provided in the two key *X*-filling operations in order to reduce capture power as much as possible.

B. Impact of X-Filling Target Selection

Generally, a test cube contains multiple *X*-bits, and different orders of selecting the target *X*-bit for each *X*-filling run often lead to different results in capture power reduction. An example is shown in Fig. 4.

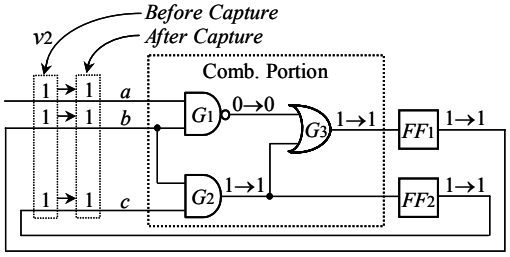


(a) Original test cube



Weighted Capture Transition Count (*v*1) = 4

(b) *X*-filling result (*Xc* first & *Xb* second)



Weighted Capture Transition Count (*v*2) = 0

(c) *X*-filling result (*Xb* first & *Xc* second)

Fig. 4. Impact of *X*-filling target selection.

As shown in Fig. 4 (a), the test cube *v* has two *X*-bits, represented by *Xb* and *Xc*, respectively. If *Xc* is *X*-filled before *Xb* with an LCP *X*-filling method [21], the resulting test vector is *v*1 and its weighted capture transition count is 4 as shown in Fig. 4 (b). The *weighted capture transition count* is an effective metric for capture power estimation as to be discussed in Section 2.3. However, if *Xb* is *X*-filled before *Xc*, the resulting test vector is *v*2 and its weighted capture transition count is 0 as shown in Fig. 4 (c). Clearly, the guidance provided in *X*-filling target selection in Fig. 4 (c) is more effective than that of Fig. 4 (b), with respect to capture power reduction.

However, previous LCP *X*-filling methods usually select an *X*-filling target in a random manner, or by a simple heuristic without a close correlation with capture power reduction [21, 22]. This lack of guidance in *X*-filling target selection adversely affects the result of capture power reduction.

C. Power Estimation for X-Filling Value Selection

After the target *X*-bit for the current *X*-filling run is selected, a proper logic value should be selected for it in order to reduce capture power as much as possible. For *X*-filling value selection, it is necessary to estimate the impacts of both 0-selection and 1-selection on capture power reduction, so as to determine which logic value, 0 or 1, is better to be used as the final logic value for the *X*-bit. Obviously, an sufficiently-accurate and easy-to-calculate metric for capture power estimation needs to be used as a guidance.

However, previous LCP *X*-filling methods lack sufficient guidance in *X*-filling value selection, with some primarily targeting shift power reduction [11] and others only considering FF transitions but ignoring gate transitions [21, 22]. Such insufficient guidance in *X*-filling value selection, especially in terms of inaccurate capture power estimation, also adversely affects the result of capture power reduction.

For a fully-specified test vector *v*, its *weighted capture transition count*, denoted by *WCT*(*v*), is a good metric for capture power estimation, as defined bellow:

$$WCT(v) = \sum_{i=1}^{n} (w_i \times t_i)$$

where *n* is the number of all nodes (gates and FFs) in a circuit, w_i is the number of fanout branches from node *i*, and t_i indicates whether a capture transition occurs at the output of node *i*. Here, $t_i = 1$ if a capture transition occurs; otherwise, $t_i = 0$. Note that w_i is used to approximate the parasitic capacitance at node *i*.

For example, consider v_1 shown in Fig. 4 (b). Since there are three capture transitions at G_1, G_3, and FF_1 that have 1, 1, and 2 fanout branches, respectively, it is obvious that

$$WCT(v_1) = 1\times1 + 1\times1 + 1\times2 = 4$$

The weighted capture transition count metric is tailored from the more general concept of *weighted switching activity* [2,12] to fit into capture power estimation. Since it takes all nodes and their fanout branches into consideration, this metric provides sufficiently-accurate estimation on capture power dissipation caused by a test vector, without resorting to costly simulation-based power analysis.

However, the weighted capture transition count is a deterministic metric. That is, it can be used only for a fully-specified test vector, not for a test cube with *X*-bits. This is because, since *X*-bits exist in a test cube, the outputs of some nodes could also be *X*'s before and/or after capture. For example, if the output of a node is *X* before capture and 1 after capture, it is impossible to deterministically know whether a capture transition occurs at the node.

Therefore, the weighted capture transition count cannot be used as a guidance in *X*-filling value selection. This is because a test cube often still has *X*-bits after one of its *X*-bits is filled with 0 or 1, but the weighted capture transition count can only be used for a test vector without *X*-bits.

D. Motivation

As discussed above, previous LCP *X*-filling methods fail to provide sufficient guidance in the key *X*-filling operations: *X-filling target selection* and *X-filling value selection*. That is, the two selections are not sufficiently guided since their impact on the capture power of a test cube is not fully taken into consideration, due to such reasons as overly-simplified selection heuristics and the lack of a sufficiently-accurate metric for estimating capture power of a test cube with *X*-bits. As a result, the performance of previous LCP *X*-filling methods is usually not satisfactory.

Therefore, there is a strong need for a highly-guided LCP *X*-filling method. This method should be able to make highly-guided decisions based on sufficiently-estimated impact on capture power reduction, in both *X*-filling target selection and *X*-filling value selection.

In the following, we propose a highly-guided LCP *X*-filling method, featuring two novel concepts: (1) *X-score* and *probabilistic weighted capture transition count*. The former is unique in that it quantifies the impact of each *X*-bit on capture power reduction, while the latter is unique in that it estimates whole-circuit capture power dissipation even for a test cube. Sufficient guidance in *X*-filling based on the two concepts leads to significant improvement in capture power reduction.

III. Overview of Highly-Guided LCP *X*-Filling

Fig. 5 shows the general overview of the new LCP *X*-filling method that provides sufficient guidance in *X*-filling, based on the concepts of the *X*-score and the probabilistic weighted capture transition count. This procedure starts from a test cube with *X*-bits, and consists of two basic operations: (1) properly selecting a target *X*-bit for each *X*-filling run, and (2) determining a proper logic value for the target *X*-bit, so as to reduce capture power as much as possible. Operations ① and ② are repeated until there are no more *X*-bits, and the result is a fully-specified test vector.

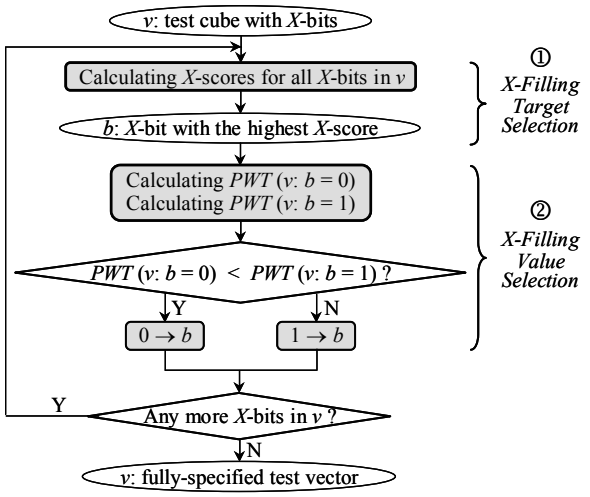


Fig. 5. Highly-guided LCP *X*-filling procedure.

As shown in Fig. 5, *X*-filling target selection is conducted by calculating the *X*-score for each *X*-bit in a test cube and then choosing the one with the largest *X*-score as the *X*-filling target for the current *X*-filling run. Details on *X*-filling target selection are provided in Section 4.

On the other hand, *X*-filling value selection for the target *X*-bit *b* in a test cube *v* is conducted by calculating the probabilistic weighted capture transition counts of both 0-selection and 1-selection for the *X*-bit *b*, denoted by *PWT*(*v*: *b* = 0) and *PWT*(*v*: *b* = 1), respectively, as shown in Fig. 5. The logic value corresponding to the smaller *PWT* value is selected as the final logic value for the target *X*-bit. Details on *X*-filling value selection are provided in Section 5.

IV. *X*-Filling Target Selection

In order to properly select the *X*-filling target for the current *X*-filling run, it is necessary to consider the following factors: (1) the circuit structure, (2) the values and locations of specified bits, and (3) the locations of *X*-bits. Information on these factors is obtained by a technique called *set-simulation*, which is an extension to the *X*-simulation technique [26]. *X*-score is then calculated from the result of set-simulation, and used to guide *X*-filling target selection.

A. Set-Simulation

Set-simulation is conducted for a test cube *v* in a full-scan circuit by using the following procedure:

Set-Simulation

Step-1: Input Set Assignment

Suppose that the test cube *v* has *n X*-bits. Replace the *n X*-bits with *n* different sets: {1}, {2}, ..., and {*n*}.

Step-2: Set Propagation

Conduct set propagation in the combinational portion of the full-scan circuit until the output of each gate has either a logic value or a set, by repeatedly applying Rules I and II:

Rule-I: If the output of a gate is the inversion of one of its inputs and the input has the set *S* ($\overline{S}$), then place $\overline{S}$ (*S*) on the output of the gate.

Rule-II: Suppose that a total of *p* inputs of a gate have sets S_1, S_2, ..., and S_p. If the output of the gate is neither a logic value nor the inversion of any of its inputs, place the set $S_1 \cup S_2 \cup ... \cup S_p$ on the output of the gate.

Step-3: FF Set Assignment

After a logic value or a set is determined at a pseudo primary output of the combinational portion, assign the logic value or the set of the pseudo primary output to the output of its corresponding FF. □

An example of set-simulation is shown in Fig. 6. Generally, set-simulation for a test cube reveals the impact of each *X*-bit on logic values of nodes as follows: (1) a logic value on the output of a node indicates that no *X*-bit has any impact on the node, and (2) a set $\{p_1, p_2, ..., p_m\}$ on the output of a node indicates that the logic value of the node is affected by the p_1-th *X*-bit, the p_2-th *X*-bit, ..., and the p_m-th *X*-bit in the test cube. This information is used in calculating *X*-scores.

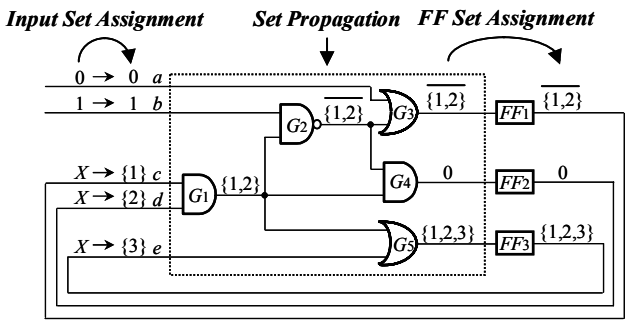


Fig. 6. Set-simulation.

B. X-Score Definition

Definition 1: Suppose that the outputs of a total of *m* nodes (gates and FFs) in a full-scan circuit have sets of numbers, S_1, S_2, ..., and S_m, after set-simulation is conducted for a test cube. Also suppose that n_{bit} is the number assigned to an *X*-bit *bit* in the test cube in the Step-1 (Input Set Assignment) of the set-simulation procedure. In this case, the *X-score* of the *X*-bit *bit* is defined as follows:

$$X\text{-}Score(bit) = \sum_{i=1}^{m} (r_i / |S_i|)$$

where $r_i = 1$ if $n_{bit} \in S_i$; otherwise, $r_i = 0$.

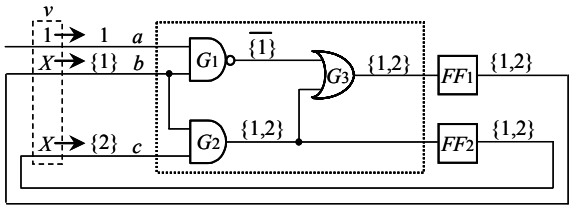
For example, for the result of set-simulation shown in Fig. 6, the outputs of nodes G_1, G_2, G_3, G_5, FF_1, and FF_3 have sets {1,2}, $\overline{\{1,2\}}$, $\overline{\{1,2\}}$, {1,2,3}, $\overline{\{1,2\}}$, and {1,2,3}, respectively. In addition, the number 3 is assigned to the *X*-bit *e* in the Step-1 of set-simulation. Therefore, the *X*-score of the *X*-bit *e* can be calculated as follows:

$$X\text{-Score}(e) = 0/2 + 0/2 + 0/2 + 1/3 + 0/2 + 1/3 = 0.67$$

From the definition of *X*-score, it is clear that the larger the *X*-score of an *X*-bit, the more impact assigning a logic value to the *X*-bit has on the values of nodes in a full-scan circuit. Thus, an *X*-bit with a larger *X*-score indicates that the *X*-bit has more impact on capture power dissipation.

C. X-Filling Target Selection Method

As shown in Fig. 5, the proposed *X*-filling target selection method first calculates the *X*-scores of all *X*-bits in a test cube, and then selects the *X*-bit with the highest *X*-score as the *X*-filling target for the current *X*-filling run. The effect of using *X*-scores as guidance is illustrated in Fig. 7.



X-Score(*b*) = 1 + 1/2 + 1/2 + 1/2 + 1/2 = 3
X-Score(*c*) = 1/2 + 1/2 + 1/2 + 1/2 = 2

Fig. 7. *X*-filling target selection based on *X*-scores.

The circuit and the test cube shown in Fig. 7 are the same as those shown in Fig. 4 (a), respectively. The test cube v has two X-bits on b and c. As shown in Fig. 7, X-score(b) and X-score(c) are 3 and 2, respectively. Therefore, b is selected as the first target X-bit for X-filling, and c is the second. As already shown in Fig. 4 (b) and (c), this order of X-filling leads to a better result in capture power reduction.

V. X-Filling Value Selection

In order to reduce capture power as much as possible, a proper logic value needs to be selected for the target X-bit in each X-filling run. Determining whether a logic value is proper for an X-bit in the process of X-filling requires sufficiently-accurate estimation on capture power for a test cube with X-bits. In the following, a new metric is defined for capture power estimation of a test cube, and details on its calculation are also described. Based on the new metric, highly-guided X-filling value selection is achieved.

A. Probabilistic Weighted Capture Transition Count

Definition 2: The ***probabilistic weighted capture transition count*** of a circuit for the capture operation under a test cube v is denoted by $PWT(v)$ and defined as follows:

$$PWT(v) = \sum_{i=1}^{n} (w_i \times p_i)$$

where n is the number of all nodes (gates in the combinational portion and FFs in the scan chains) of the circuit, w_i is the number of fanout branches from node i, and p_i is the probability that a transition ($0\rightarrow1$ or $1\rightarrow0$) occurs at the output of node i.

Obviously, the probabilistic weighted capture transition count (PWT) is similar to the weighted capture transition count (WCT) described in Section 2.3. The most significant difference is that PWT uses the concept of transition probability to handle un-deterministic transitions associated with X-bits in a test cube, while WCT can only handle deterministic transitions for a fully-specified test vector.

For example, if the output of a node is X before capture and 1 after capture, it is impossible to determine whether a transition ($0\rightarrow1$) will occur at this node with 100% certainty. In order to address this uncertainty, the concept of *transition probability* is introduced. Generally, the transition probability p_i at node i for the capture operation under a test cube v can be calculated by

$$p_i = (BC\text{-}Prob^0(i) \times AC\text{-}Prob^1(i)) + (BC\text{-}Prob^1(i) \times AC\text{-}Prob^0(i))$$

where $BC\text{-}Prob^0(i)$ and $BC\text{-}Prob^1(i)$ denote the probabilities of node i having 0 and 1 *before capture* (*BC*), respectively, while $AC\text{-}Prob^0(i)$ and $AC\text{-}Prob^1(i)$ denote the probabilities of node i having 0 and 1 *after capture* (*AC*), respectively. This is illustrated in Fig. 8.

Once transition probabilities of all nodes for v are obtained, $PWT(v)$ can be calculated. The significant benefit of the PWT metric is its capability to estimate capture power of the whole circuit even for a test cube. This makes it useful in guiding X-filling value selection to effectively reduce capture power.

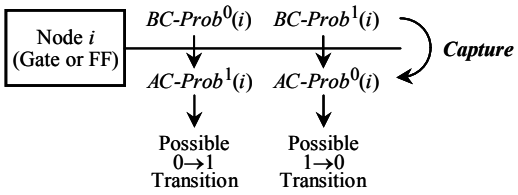


Fig. 8. Concept of transition probability.

The key issue in applying the PWT metric is to obtain the transition probabilities of all nodes under a test cube v. As shown in Fig. 8, this requires to calculate four *node probabilities*, $BC\text{-}Prob^0(i)$, $BC\text{-}Prob^1(i)$, $AC\text{-}Prob^0(i)$, and $AC\text{-}Prob^1(i)$, for each node i. Although $BC\text{-}Prob^0(i) + BC\text{-}Prob^1(i) = 1$ and $AC\text{-}Prob^0(i) + AC\text{-}Prob^1(i) = 1$, all the four probabilities are explicitly shown for each node in the following for the ease of comprehension.

The probabilities of all nodes under a test vector v can be calculated in the following four steps as illustrated in Fig. 9, corresponding to the full-scan circuit shown in Fig. 1.

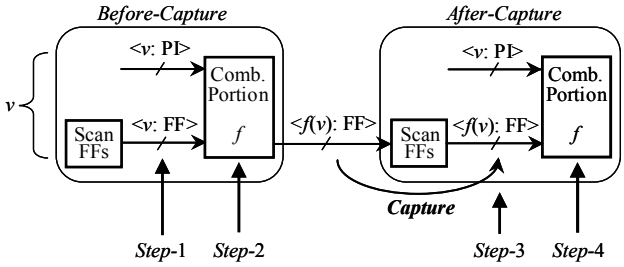


Fig. 9. Node probability calculation.

Node Probability Calculation

Step-1: Before-Capture Input Probability Assignment

The before-capture 0 and 1 probabilities of each bit b in the test cube v are assigned according to its value as follows:

TABLE I
Before-Capture Input Probability Assignment Rules

b	$BC\text{-}Prob^0(b)$	$BC\text{-}Prob^1(b)$
0	100%	0%
1	0%	100%
X	50%	50%

Step-2: Before-Capture Node Probability Calculation

The before-capture 0 and 1 probabilities of each gate in the combinational portion are calculated from the input probabilities assigned in Step-1. Many methods are available for probability propagation [27-29], with different trade-offs between correlation-induced inaccuracy and computational complexity. Note that the before-capture 0 and 1 probabilities of each FF have been assigned in Step-1.

Step-3: After-Capture Input Probability Assignment

The effect of the capture operation is to update the outputs of scan FFs with <$f(v)$: FF>, which is the response of the combinational portion to the test cube v at the inputs of the FFs.

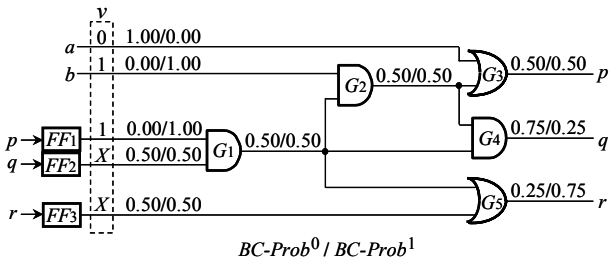
Thus, the after-capture 0 and 1 probabilities of the output of each FF are equal to the before-capture 0 and 1 probabilities of the input of the FF, respectively. The values of primary inputs <*v*: PI> remain unchanged by capture. Thus, the after-capture 0 and 1 probabilities of each primary input remain unchanged from its corresponding before-capture 0 and 1 probabilities, respectively.

Step-4: After-Capture Node Probability Calculation

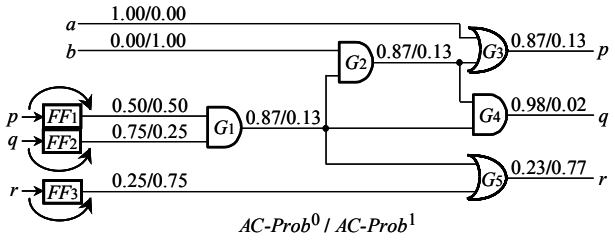
The after-capture 0 and 1 probabilities of each gate in the combinational portion are calculated from the input probabilities assigned in Step-3. Note that the after-capture 0 and 1 probabilities of each FF have already been assigned in Step-3. □

It is clear that in Step-1, any *X*-bit in a test cube *v* can be set to any logic value directly from primary inputs or indirectly through scan shift. This is why the 0 and 1 probabilities for any *X*-bit in a test cube are assigned to 50%.

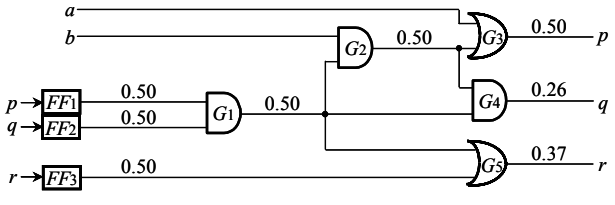
An example of calculating node and then transition probabilities is shown in Fig. 10. The full-scan circuit has a combinational portion of five gates ($G1 \sim G5$) and three scan FFs ($FF1 \sim FF3$). *a* and *b* are primary inputs, while *p*, *q*, and *r* are pseudo primary outputs that are connected to the inputs of $FF1$, $FF2$, and $FF3$, respectively.



(a) Before-capture node probabilities



(b) After-capture node probabilities



(c) Transition probabilities

Fig. 10. Node and transition probability calculation.

Fig. 10 (a) and (b) show before-capture and after-capture node probabilities, respectively. From these results, it is easy to calculate transition probabilities for all nodes as illustrated in Fig. 8, and the result is shown in Fig. 10 (c). Therefore, $PWT(v) = 3\times0.50 + 2\times0.50 + 1\times0.50 + 1\times0.26 + 1\times0.37 + 1\times0.50 + 1\times0.50 + 1\times0.50 = 5.13$.

B. X-Filling Value Selection Method

As shown in Fig. 5, in order to select a proper logic value for an *X*-bit *b* in a test cube *v* for capture power reduction, one first calculates $PWT(v: b = 0)$ and $PWT(v: b = 1)$, denoting the probabilistic weighted capture transition counts for the cases of assigning 0 and 1 to *b*, respectively. Then one selects the logic value corresponding to the smaller PWT value as the final value for the *X*-bit *b*.

Since the probabilistic weighted capture transition count can estimate capture power dissipation at all nodes (gates and FFs) for a test cube with *X*-bits, the *X*-filling value selection based on this metric is a highly-guided procedure, leading to a better result in capture power reduction.

VI. Experimental Results

A. Comparison

X-filling experiments were conducted on ISCAS'89 circuits for typical *X*-filling methods [11, 12, 21, 22], namely random filling (*Ran.*), 0-filling (*0-fill*), 1-filling (*1-fill*), minimum-transition-filling (*MT*) [11], and minimum-FF-transition filling (*FF*) [21], in order to compare them with the highly-guided LCP *X*-filling method (*New*) proposed in this paper. The results are summarized in Table 2.

TABLE II
Comparison of *X*-Filling Methods

Circuit	Test Vec. #	Fault Cov. (%)	Initial Max. WCT	*X* (%)	Max. WCT Reduction Ratio (%)					
					Ran.	*0-Fill*	*1-Fill*	*MT*	*FF*	*New*
s1196	115	100	110	56.8	0.0	-10.9	10.0	-10.0	30.9	**30.9**
s1238	125	94.9	121	57.1	9.9	3.3	0.8	0.8	32.2	**50.4**
s1423	24	99.1	648	43.1	4.9	20.2	-5.6	-2.8	11.1	**24.5**
s5378	101	99.1	2219	73.5	-1.8	-5.9	-27.1	-25.2	22.9	**29.7**
s9234	108	93.5	3822	69.0	5.8	22.4	5.3	5.2	24.9	**33.4**
s13207	236	98.5	5238	91.4	10.2	19.8	0.4	12.4	21.7	**33.7**
s15850	94	96.7	4438	77.3	1.6	20.6	-15.4	4.8	20.7	**36.3**
s35932	13	89.8	17804	41.2	8.1	9.2	-0.8	-0.8	9.2	**12.2**
s38417	87	99.5	14183	76.8	2.8	12.4	4.4	12.9	15.7	**24.7**
s38584	118	95.9	14324	82.0	3.9	25.8	21.9	3.2	35.0	**34.1**
Ave.				66.8	4.5	11.7	-0.6	0.1	22.4	**31.0**

Table 2 shows the number of test vectors (*Test Vec. #*), the fault coverage (*Fault Cov.*), and the initial maximum weighted capture transition count (*Initial Max. WCT*) for each circuit. The XID technique [25] was used to identify *X*-bits from a fully-specified test set without fault coverage loss, and on average 66.8% of bits were found to be *X*-bits. Capture power for all nodes (gates and FFs) in a circuit after *X*-filling was estimated by the weighted capture transition count (WCT) as described in Section 2.3.

Clearly, highly-guided LCP *X*-filling proposed in this paper (*New*) performed the best among the *X*-filling methods, with an average of 31.0% reduction in capture power. Capture power

analysis was also conducted with PrimePower™ and a UMC 0.18μm library, and the results are shown in Fig. 11.

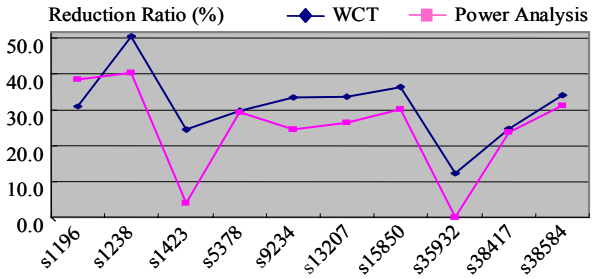


Fig. 11. Capture power analysis results.

B. Discussions

• Fig. 11 shows insignificant reduction results for s1423 and s35932. The reason is that both circuits have a inappropriately small number of test vectors and thus a small percentage of *X*-bits. In normal cases, a large percentage of *X*-bits exists, leading to high reduction ratio.

• Highly-guided LCP *X*-filling can be directly used together with test compression techniques that do not rely on *X*-bits, such as OPMISR. For test compression techniques that rely on *X*-bits, such as EDT and Virtual-Scan, trade-off is needed to balance test compression and capture power reduction. A slight increase in test data volume may occur, but it can be readily absorbed by test compression.

VII. Conclusions

This paper proposed an effective *X*-filling method for capture power reduction, based on the novel concepts of *X-score* and *probabilistic weighted capture count* for providing sufficient guidance in *X*-filling target selection and *X*-filling value selection, respectively. Experimental results demonstrated the superiority of the proposed method in reducing capture power without the need of any circuit modification. Furthermore, the basic idea of this paper can be readily extended to the double-capture clocking scheme for at-speed scan testing.

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