Fast Power Network Analysis with Multiple Clock Domains

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Abstract

This paper proposes an efficient analysis flow and an algorithm to identify the worst case noise for power networks with multiple clock domains. First, we apply the Laplace transform on the input current sources to derive the analytical formula. Then, we calculate the circuit frequency response with logarithmic scale frequency components. The frequency domain response is approximated by a rational function using vector fitting modeling. The rational function is used to derive the natural frequency of the power ground networks, and can be converted back into time domain easily. Based on the analysis results, we then present the worst case clock gating pattern algorithm to analyze the power networks with multiple clock domains. The most expensive part of the proposed algorithm is the matrix solving: $O(F(N)\cdot \log f \cdot D)$. *Function* F *is the complexity of iterative solution of complex matrix with dimension N. We assume that there are* D *clock domains and the frequency spans from 0 to* f *Hz. Experimental results show that our method is up to 60X faster than HSPICE, and can analyze large circuits which are not affordable by HSPICE.*

1. Introduction

Power ground (P/G) networks supply power from the P/G pads on a chip to the circuit modules. With the rapid increase of working frequency and continuous scaling of VLSI technology, it is becoming more and more important to analyze power networks efficiently and accurately.

For power noise simulation, two kinds of noises in power supply networks need to be identified: first the IR drop which is due to the power grid resistance, and second simultaneous switching noise which is because of the package inductance [3]. These noises will lead to adverse impacts on chip, package and board performance such as longer path delay or logic failure. The noise problem may be even worse when the frequency of input source matches the natural frequency. Therefore, circuit analysis tools need to produce the results of not only time domain voltage waveform to analyze the noise, but also natural frequency of the circuit in order to avoid resonance.

For worst case voltage variations, lots of research works have been addressed. Bai et al [1] proposed MIMAX algorithm to generate a tight upper-bound on the maximum macro-block current envelope which would lead to worst case voltage drop. Shi *et al* [9] introduced an algorithm to compute the worst case logical timing correlations among the cells leading to resonance with large voltage drops. Lin et al [7] provided a statistical vectorless dynamic supply noise analysis approach.

The noise analysis is more complicated when there are multiple clock domains, and the clock gating pattern is different in each domain. Clock gating is a technique to reduce clock power. Clock gating disables the clock to a circuit by ANDing the clock with a gate control signal when the circuit is not used to avoid unnecessary power dissipation [6]. Currently, we can simulate the whole circuit in one clock cycle to find the voltage drop in time domain. However calculating the worst case voltage variation is currently a challenge when the circuit works for several cycles and with multiple clock domains. If we can identify the worst case clock gating pattern, we only need to simulate under this pattern and obtain the worst case voltage variation. Otherwise, different possible combinations of gating pattern need to be taken into consideration, and the simulation will be time-consuming.

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Several previous works focused on the efficient time domain simulation and try to consider the large number of the nodes in the power networks. In some works the problem size is reduced by emphasizing on the circuit using methods such as circuit partitioning [5] and multigrid-like technique [8]. In others, the efficiency of the simulation is improved using numerical methods. They apply direct solver "KLU", or iterative solvers such as "Conjugate Gradient" or "Generalized Minimal Residual Method".

In this work, we propose an efficient analysis flow and an algorithm to identify the worst case clock gating pattern in order to improve the efficiency of the power networks simulation and identify natural frequency. Our contributions are:

(1) Apply Laplace transform to the piecewise linear (PWL) input sources to derive the analytical formulation, and compute the spectrum in the frequency domain efficiently.

(2) Use the logarithmic scale for sampling the frequency components in order to accelerate the wide spectrum analysis.

(3) Propose a vector fitting based method to approximate the frequency domain response and calculate the time domain results efficiently. The new algorithm requires less sampling data in the frequency domain, and fits these data to be a rational function. Natural frequencies can be easily computed from the rational function. We also derive analytical formulation to convert frequency response back into the time domain.

(4) Propose an algorithm to identify the worst case clock gating pattern with multiple clock domains based on superimposition.

We discuss the problem statement and algorithm overview in section 2 and 3 respectively. In section 4, we introduce the vector fitting based simulation method, and explain the complete flow. The worst case clock gating algorithm is discussed in section 5. Section 6 describes the analysis of the computational complexity of the proposed algorithm. Section 7 depicts the experimental results. The last section is our conclusions and future works.

2. Problem Statement

Power networks consist of resistance, capacitance and inductance components as shown in figure 1, which have multiple resonance frequencies. Time-varying current sources are adopted to model the non-linear effect of the active transistors connected to the power networks. These current sources draw (sink) current from (to) power networks and cause voltage fluctuations in the P/G network.

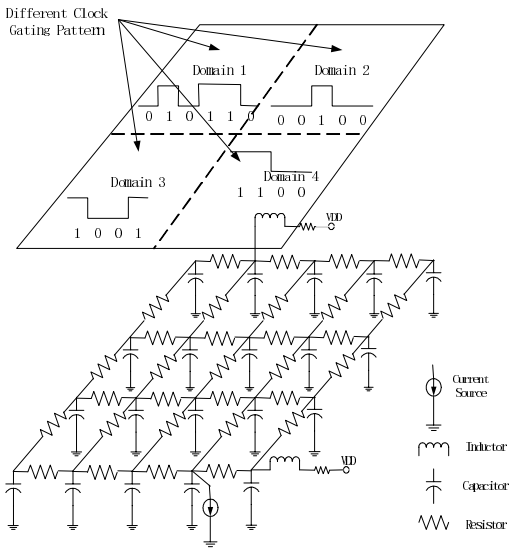

Figure 1. Power supply network modeling

The power networks consist of multiple clock domains. All the transistors in the same domain switch synchronously. The clock domains are independent from each other. The clock gating pattern is the controlling signal. As shown in figure 1, "1" represents the transistors are switching in this cycle while "0" represents the sleep mode. Therefore, our main goal is to determine the clock gating patterns in each domain in order to achieve the worst case voltage variations. To make the analysis more efficient, we also propose an analysis flow based on the vector fitting.

Here are our assumptions during the analysis flow:

(1) The power networks are arbitrary RLC circuits, and the current sources are given.

(2) The current sources in each clock domain are determined by vectorless approach [7] which will lead to the peak noise. In other words, we assume that the current sources are the same in every cycle for each clock domain when it is not gated.

(3) Each clock domain has its own independent clock gating pattern. Note that if the current sources are different at different cycle, we may divide them between different clock domains.

3. Overview

We solve the worst case noise analysis problem with two steps. First, we apply the proposed simulation method with each clock domain working for one cycle. Second, with the simulation results of each clock domain, we propose an algorithm to find the worst case clock gating if all the domains are working together independently.

Figure 2 illustrates the flow of the analysis. The system inputs the power networks and the current sources of each clock domain and outputs the worst voltage drop and the corresponding clock gating pattern. In the first stage, we simulate the output waveform of each clock domain. The second stage combines the output waveforms of all clock domains to derive the worst voltage drop.

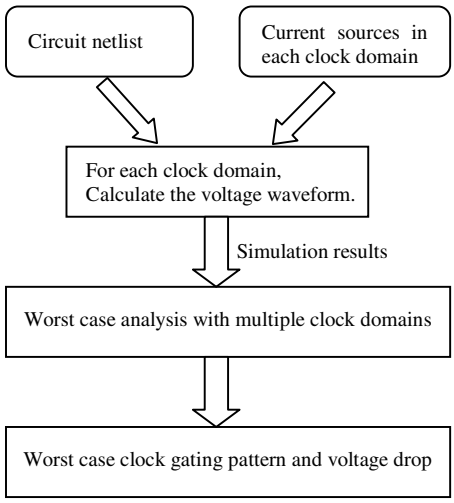

Figure 2. The whole analysis flow

4. Simulation using Vector Fitting Method

We use the vector fitting method to calculate the output voltage of each clock domain. Figure 3 describes the flow for the time domain response computation. The core engine operates in the frequency domain which enables us to compute the natural frequencies of the system behavior.

We first convert the current sources from time domain to frequency domain representation. We assume that the input I(t) is described as piecewise linear (PWL) function. We thus can use Laplace transform to derive the frequency domain formulation I(s). Then, we solve the complex matrix to compute the frequency domain voltage response. We adopt vector fitting to approximate the discrete sampling output voltages V(s) with rational functions. Finally, we convert the voltage V(s) in partial fractional expression to time domain representation V(t).

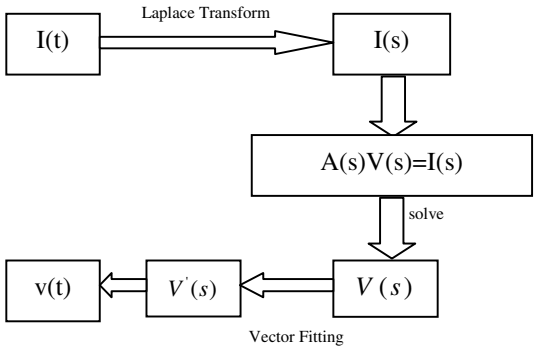

Figure 3. Proposed simulation algorithm for voltage response

4.1. Laplace transform of input sources

We apply Laplace transform to the PWL input current sources. Let us denote the ramp function as

$$R(t) = t \cdot u(t) . \quad (1)$$

where $u(t)$ is the unit step function. The Laplace transform of a ramp function is

$$R(s) = 1/s^2 \quad (2)$$

We superpose the ramp functions to express the current sources (Fig. 4) in time domain.

$$f(t) = \sum_i a_i R(t - t_i) \qquad f(t) = 0 \text{ for } t \geq T , \quad (3)$$

where a_i is the slope difference between the current curve and the previous curve. T is the period of this current source. Applying the Laplace transform, we convert function $f(t)$ to *s* domain representation:

$$F(s) = \sum_i \frac{a_i \cdot e^{-s \cdot t_i}}{s^2} \quad (4)$$

When $s = 0$, the DC value is the area of the input current source.

4.2. Frequency domain matrix solving

We use logarithmic scale to sample the output in frequency domain. The voltage V(s) is calculated by solving a simultaneous linear equation:

$$A(s) \cdot V(s) = I(s) , \quad (5)$$

where A(s) is the complex admittance matrix of the circuit, V(s) is the vector of voltage at each node and I(s) is the input current source vector. We apply the Conjugate Gradient Square (CGS) method with

Incomplete LU (ILU) as preconditioner to solve the complex matrix.

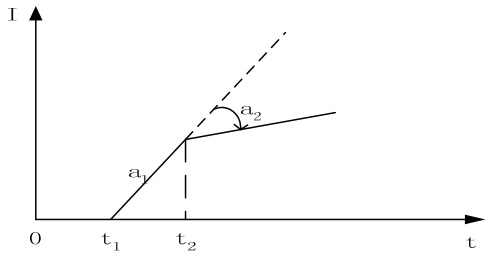

Figure 4. Piecewise linear current source

4.3. Vector fitting method

We use vector fitting (VF) method to fit the sampled output voltage V(s) with a rational expression [4]. We use partial fractional expression

$$F(s) = \sum_{n=1}^{N} \frac{c_n}{s - a_n} + d + sh \qquad (6)$$

where the residues C_n and poles a_n are either real numbers or complex conjugate pairs, parameters d and h are real.

The most expensive computation section is to solve the simultaneous equations based on singular value decomposition (SVD). For a dense $p \times q$ matrix, SVD is usually computed by $O(pq^2 + p^2q + q^3)$ [2]. In vector fitting, p is equal to the number of sampling data, and q is $2h+2$, where h is the number of initial poles. Usually, the number of sampling data is larger than h. Therefore, the complexity of vector fitting is $O(K^2h)$ where K is the number of sampling data.

The time domain response is derive from function (6) via inverse Laplace transform.

$$f(t) = \sum_{n=1}^{N} [c_n \cdot e^{a_n t} \cdot u(t)] \qquad (7)$$

5. Worst Case Clock Gating Algorithm

In this section, we will explain the algorithm for identifying the worst case clock gating pattern with multiple clock domains. The voltage waveform may not return to 0 at the end of one clock cycle, and therefore the voltage variation may be even worse in several cycles.

The idea which we propose in this section is based on the superposition. Suppose the current source $f(t)$ in one clock cycle, and then the current with clock gating for k cycles can be expressed as

$$g(t) = \sum_{i=0}^{k-1} b_i f(t - iT) \qquad (8)$$

where $b_i = 1$ means clock domain is functioning, while $b_i = 0$ means the clock domain is gated.

The frequency transform of the current is:

$$G(s) = F(s) \sum_{i=0}^{k-1} (b_i \cdot e^{-siT}) \qquad (9)$$

Therefore, the output is:

$$Y(s) = H(s)G(s) = [H(s)F(s)] \sum_{i=0}^{k-1} (b_i \cdot e^{-siT}) \qquad (10)$$

where $H(s)F(s)$ is the frequency response in one clock cycle. Because of the linear phase of $\sum_{i=0}^{k-1} (b_i \cdot e^{-siT})$, the time domain response is:

$$\sum_{i=0}^{k-1} b_i \cdot y(t - iT) \qquad (11)$$

where $y(t)$ is the voltage response for the input $f(t)$, and can be computed by the proposed simulation method.

We superimpose all the positive voltage to derive the worst case. The situation is similar for all the negative voltage variations. In each clock cycle, the clock gating pattern which corresponds to the largest variation among all the positive and negative variations is considered as the worst case. Figure 5 is the parameters description for the worst case clock gating pattern algorithm, which is presented in figure 6.

The input of the proposed simulation method is the piecewise linear current sources in one clock cycle. The goal of the proposed algorithm is to identify whether the current waveforms are repeated or sleeping in the following cycles.

The simulation result $y_i(t)$ is the transient response of clock domain i and will span multiple cycles due to resonance.

For each clock domain i, we construct a positive function $y_i^P(t)$ and a negative function $y_i^N(t)$. Then we superimpose these two functions to be $\sum_{j=0}^{C_i-1} y_j^P(t - jT)$ and $\sum_{j=0}^{C_i-1} y_j^N(t - jT)$ respectively.

D: the number of clock domains

Positive function $y_i^P(t) = y_i(t)$ when $y_i(t) > 0$

= 0 when $y_i(t) \le 0 \ \forall i \in \{1,2,...,D\}$

Negative function $y_i^N(t) = y_i(t)$ when $y_i(t) \le 0$

= 0 when $y_i(t) > 0 \ \forall i \in \{1,2,...,D\}$

P(t): the superimposing curve of $y_i^P(t)$ in all of clock domain i

N(t): the superimposing curve of $y_i^N(t)$ in all of clock domain i

$P_G[i][j]$: the clock gating pattern for the positive voltage variation at i^{th} domain and j^{th} cycle, where "1" represents working and "0" represents gated.

$N_G[i][j]$: the clock gating pattern for the negative voltage variation at i^{th} domain and j^{th} cycle, where "-1" represents working and "0" represents gated.

Figure 5. Parameters description for worst case clock gating pattern algorithm

The superposition for all the D clock domains are:

$$P(t) = \sum_{i=1}^{D} \sum_{j=0}^{C_i - 1} y_j^P(t - jT)$$

$$N(t) = \sum_{i=1}^{D} \sum_{j=0}^{C_i - 1} y_j^N(t - jT)$$

At this stage, we find the time point t_{MP} corresponding to the maximum value of $P(t)$. We set the clock to be functioning in j^{th} cycle if $y_i^P(t_{MP} - jT) > 0$, and gated otherwise. We follow the same process for the negative voltages, $N(t)$, to derive the worse case clock gating pattern. Here we assume that $V_{DD} = 0$.

6. Complexity Analysis

We analyze the time complexity of each step in the proposed algorithm.

(1) The complexity of the Laplace transform on input current sources is: $O(n_s n_t \log f)$. Here n_t is the number of terms in PWL current source and n_s is the number of current sources. The frequency range is f, and therefore, the number of the sampling components is $\log f$.

(2) The complexity of matrix computation is: $O(F(N) \cdot \log f \cdot D)$. Here, function F is the complexity of ILU+CGS and the matrix solver requires

Algorithm objective: To identify the worst case clock gating pattern for the power networks with multiple clock domains

1 For each clock domain i:

2 Compute the response $y_i(t)$ for only the sources in this clock domain

3 Each $y_i(t)$ takes C_i cycles to reach saturated state

4 Construct two curves $y_i^P(t)$ and $y_i^N(t)$ from each $y_i(t)$

5 Superimposing positive function $y_i^P(t)$, $y_i^P(t-T)$ … $y_i^P(t-(C_i-1)T)$, and the same for negative function $y_i^N(t)$

6 End for

7 Superimpose all of the clock domains together, we obtain the most positive and negative functions

$$P(t) = \sum_{i=1}^{D} \sum_{j=0}^{C_i - 1} y_j^P(t - jT)$$

$$N(t) = \sum_{i=1}^{D} \sum_{j=0}^{C_i - 1} y_j^N(t - jT)$$

8 Find the worst time point t_{MP}, and the worst positive voltage variation $P(t_{MP}) = \max(P(t))$

9 $P_G[i][j]$=1 when $y_i^P(t_{MP} - (j-1)T) > 0$

=0 when $y_i^P(t_{MP} - (j-1)T) = 0$

10 Find the worst time point t_{MN}, and the worst negative voltage variation:

$N(t_{MN}) = \max(abs(N(t)))$

11 $N_G[i][j]$=-1 when $y_i^N(t_{MN} - (j-1)T) < 0$

= 0 when $y_i^N(t_{MN} - (j-1)T) = 0$

12 The gating pattern corresponds to the max of $P(t_{MP})$ and $N(t_{MN})$ is the worst case pattern.

Figure 6. Proposed algorithm for the worst case clock gating pattern

$O(N)$ computation for each iteration. Variable D is the number of clock domains.

(3) The time complexity of transforming voltage V(s) to V(t): $O(\log N \cdot h \cdot (\log f)^2 \cdot D)$ which is based on the vector fitting complexity. h is the number of initial poles in the vector fitting method.

(4) The complexity of the worst case clock gating pattern algorithm is $O(\log N \cdot h \cdot k \cdot P \cdot D)$. Variable P is the number of time components of the time domain waveform that we compute in one clock cycle.

The bottleneck is the matrix solving in the second step. The proposed simulation method is efficient, because it requires less times for equation solving compared to traditional method.

7. Experimental Results

We write a C program using PETSc package to solve equation (5) for the frequency domain simulation. We choose CGS with ILU as preconditioner. Logarithmic sampling and frequency components approximation are implemented in Matlab with vector fitting package. The worst case clock gating algorithm is implemented in Matlab with the results from the efficient simulation. The C programs and HSPICE run in a Linux environment with 3GB memory and 3.2GHz Pentium 4 CPU.

Table 1. Comparison of HSPICE and proposed algorithm in time domain simulation

Circuit	# nodes	Time of HSPICE (s)	Time of proposed method (s)	Speedup
Ckt1	5678	74.6	3.5	21.3
Ckt2	11479	303.6	7.9	38.4
Ckt3	23011	873.7	16.8	52
Ckt4	46090	2033.2	34.3	59.3
Ckt5	92155	NA	84.8	NA
Ckt6	369963	NA	444.2	NA
Ckt7	1156204	NA	1976.8	NA

Table 1 lists seven test cases of power networks with mesh structures. The number of circuit nodes ranges from five thousands to over one million.

7.1. Proposed simulation method

Figure 7 illustrates the vector fitting results for one output voltage. The blue solid line is the original curve, while the red dashed line is the fitted curve. The Root Mean Square Error (RMSE) between the two curves is 8.87e-16 which shows that the vector fitting algorithm is accurate to fit the sampling data to be a rational function. Figure 8 demonstrates that the proposed simulation method approaches HSPICE result.

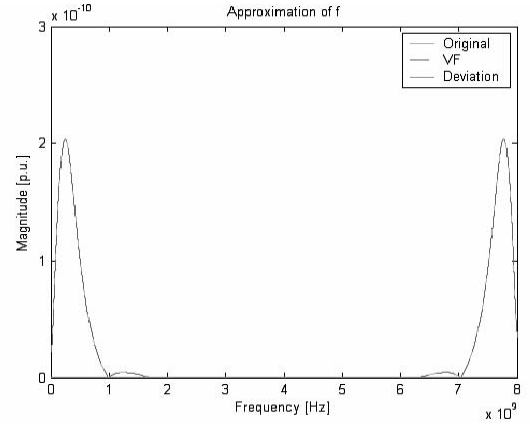

Figure 7. Vector fitting for the sampling frequency components

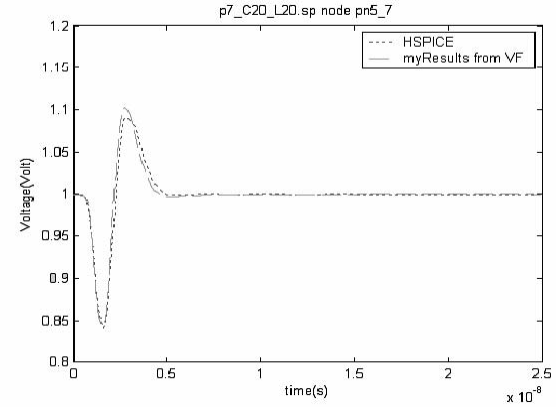

Figure 8. Comparison of HSPICE and proposed simulation algorithm

We compare the simulation time of the proposed method and HSPICE in Table 1. The running time for our program is the computation time of the frequency domain. There is an additional 0.2 sec for the vector fitting on one interested node which runs in Matlab. We make several observations based on the results shown in Table 1.

(1) Our method is up to 60 times faster than HSPICE. The speedup is even more dramatic for larger test cases.

(2) The proposed method can handle large circuits with millions of nodes. In contrast, HSPICE is not able to produce any results due to the computation ability and memory limitation for large test cases.

Second, we show the results of the computation of the transfer function and natural frequency. We apply one unit impulse input current source at each node. After solving equation (5) in frequency domain with logarithmic scale, we obtain the frequency response at

each node. Then, we apply vector fitting to the transfer function to compute the natural frequencies.

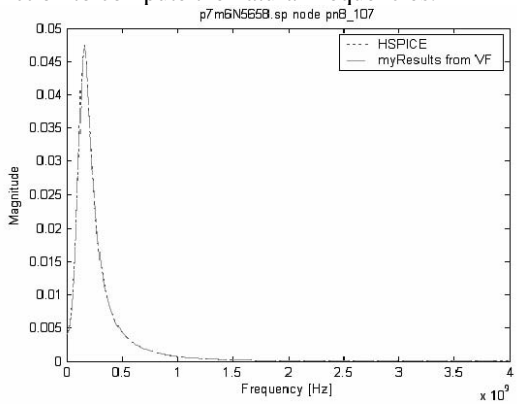

Figure 9. Comparison of HSPICE and proposed flow to compute transfer function

We compare the transfer function which is computed by HSPICE and our proposed simulation method in figure 9. The test case is a mesh power network with 5658 nodes. The red dotted line is the AC analysis result from HSPICE, while the green dashed line is from the proposed method. The vector fitting RMSE is 2.56e-7. From figure 9, we illustrate that the derived transfer function approaches the result of HSPICE. Experimental results from the proposed algorithm also identify the natural frequency to be at 160.7MHz based on the computation of the poles.

7.2. Worst clock gating with multiple clock domains

We analyze the mesh power network with four clock domains. The current sources are uniformly distributed in the same clock domain and are synchronized with each other. The clock frequency is 200MHz and the voltage response takes six cycles to reach the steady state. The four curves in figure 10 represent the voltage responses with one clock domain working for one cycle while the current sources in other three domains are gated. The node which we are concerning here is at the center of domain 1.

Table 2 lists the result of each individual clock domain and the worst case of multiple clock domains. The second column describes the peak of the voltage in response to one cycle input. The third column shows the worst case created by chosen clock gating patterns. The last column depicts the clock gating patterns. The first four rows demonstrate the result of each clock domain. For example, in domain 1, the peak voltage variation in response to one clock cycle input is -0.105V. Suppose we choose a gating pattern -1 -1 -1 0 -1 -1, the voltage drops by 0.118V. Therefore, with clock gating, the variations are worse than one single clock cycle. The last row of table 2 displays the result of four clock domains. The voltage drop 0.157V is worst than the result of single clock domain.

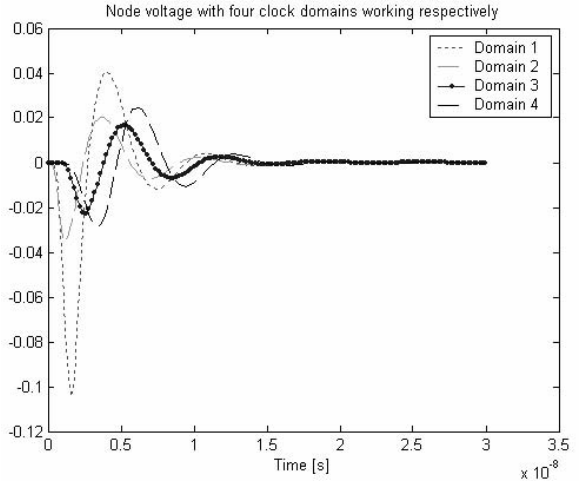

Figure 10. Voltage responses for each domain working respectively

Table 2. Worst case variations with each domain working respectively

	Waveform peak (V)	Worst case variation (V)	Worst case pattern
Domain 1	-0.105	-0.118	-1 -1 -1 0 -1 -1
Domain 2	-0.0356	-0.0406	-1 -1 -1 0 -1 -1
Domain 3	-0.0226	-0.0268	-1 -1 -1 -1 -1 -1
Domain 4	-0.0286	-0.0347	-1 -1 -1 -1 -1 -1
All domains	NA	-0.157	0 -1 -1 -1 0 -1 0 -1 -1 -1 0 -1 -1 -1 -1 0 -1 -1 -1 -1 -1 0 -1 -1

Figure 11 shows the effect of superimposing four clock domains together. The 24 rows of voltage curve are grouped into four clock domains. For each clock domain, 6 rows cover the voltage shifted in 6 clock cycles. For example, the sixth row is the sixth cycle of the voltage response. We set pattern $P_G[i][j]$ and $N_G[i][j]$ according to the waveform in each clock cycle *j*.

8. Conclusion

We proposed a worst case clock gating pattern algorithm for power networks with multiple clock domains based on an efficient power networks simulation method. The proposed method not only provides an

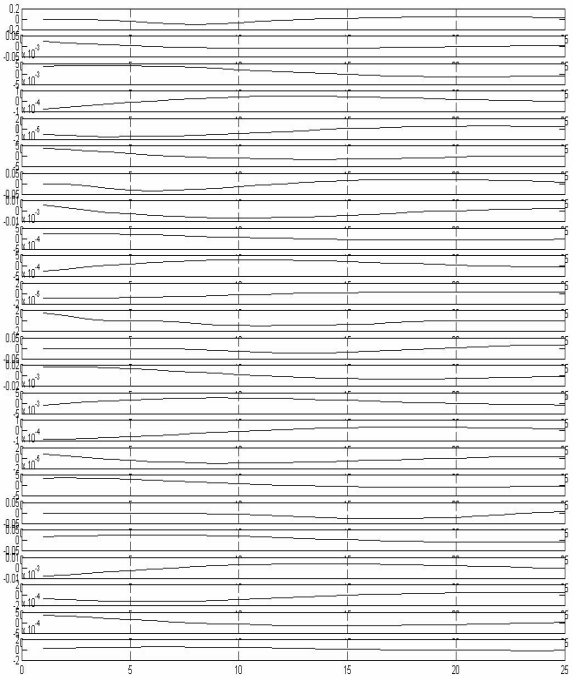

Figure 11. Superimposing of four clock domains

accurate time domain simulation, but also computes the transfer functions and natural frequencies.

The advantages of the proposed algorithm are as follows. First, we introduced an algorithm to identify the clock gating pattern for the worst case voltage variation. Second, we propose a different way to perform the time domain analysis via frequency domain responses. Third, the proposed algorithm is up to 60 times faster than HSPICE for circuit simulation, and could handle large cases. Finally, the method identifies natural frequencies in the transfer function.

Possible future work includes the parallel processing of the simulation algorithm because the frequency domain computation does not rely on the previous frequency components.

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