Power Variations of Multi-Port Routers in an Application-Specific NoC Design : A Case Study

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Abstract

In this research, we analyze the power variations present in a router having varied number of ports, in a Networks-on-Chip. The work is divided into two sections, projecting the merits and shortcomings of a multi-port router from the aspect of power consumption. First, we evaluate the power variations present during the transfers between various port pairs in a multi-port router. The power gains achieved through careful port selection during the mapping phase of the NoC design are shown. Secondly, through exhaustive experimentation, we discuss the IR-drop related issues that arise when using large multi-port routers.

1 Introduction

Networks-on-Chip (NoC) is an emerging form of system integration that is projected to meet the growing communication demands for future System-on-Chips [14]. Contrary to shared-bus that needs long & parallel interconnects, the selling points of the NoCs are better predictability for performance (owing to shorter links), modularity and scalability [12]. Being a shared network, a Networks-on-Chip suffers from several overheads including additional area, hop-based communication adding to the overall delay, congestion and tighter bandwidth constraints. Competent designs to improve the area overhead and performance are available in the literature [5, 3], wherein the stress is on the application-specific topology generation and core mapping. The router nodes are custom-tailored in order to satisfy the performance and bandwidth constraints, ignoring the ill-effects on the power front. NoCs consume a significant percentage of the total system power, thereby requiring power-efficient techniques [22, 27, 26].

Objective 1: In this research, we attempt to improve the power efficiency by exploiting the intra-port variations in power present in a multiport router (the ad-hoc switch catered to the application at hand [21, 19]). Owning to space constraints, we present the results from a five port router and highlight the power savings that can be obtained by careful selection of ports during mapping of cores.

In addition to the router architecture, topology generation and mapping form an important phase of an NoC design, having a direct impact on the final System-on-Chip performance [17]. Though it is possible to achieve a mapping that is efficient in terms of performance and power [15], ad-hoc router design and topology generation will give rise to a larger crossbar (the key element inside router), possibly resulting in larger IR drops [4]. Violations in terms of a larger current drawn will lead to timing issues and electromigration, eventually resulting in chip failures [11]. Thus, in the nanometer regime of system design, ensuring power integrity is of utmost importance, due to the widespread appearance of IR drop and ground bounce [25, 32].

Objective 2: We experiment exhaustively to observe the effect of adding ports to a router (in other words, increasing the complexity of the router) in terms of the average power variation and IR violations created. The results indicate that a large multi-port router is not beneficial from the viewpoint of power integrity.

The rest of the paper is organized as follows: Section 2 summarizes the related works. We present the details of the experimentation platform in Section 3. Section 4 discusses the power variations present between the various ports and projects a power-efficient mapping on a per router node basis. Issues on the IR drop front by the use of large multi port router are discussed in Section 5. Finally, the conclusions are summarized in Section 6.

2 Related Work

A gradual shift towards the ad-hoc design of routers, tailored to the application(s) to be interconnected through the NoC backbone is gaining prominence. In contrast to total ad-hoc designs that route packets along any desired path, we have structured implementations that introduce a heterogenous composition of routers having multiple ports [21]. Apart from the efficient router designs, topology generation and final mapping determine the efficiency of the NoC in terms of both power and performance [15, 22].

With larger System-on-Chips, NoCs are found to be consuming a significant percentage of total system power, being as high as 40% [27, 13]. Several techniques that target power reduction by optimizing the packet traffic [9]. An

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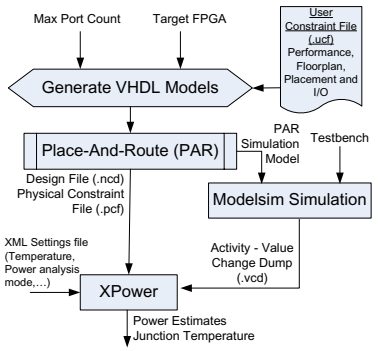


Figure 1. Xilinx FPGA flow

energy model and a buffer-reduction based energy-efficient NoC is given in [31]. Several techniques like wire-style and topology optimization [30], selective long-link insertion [18] and voltage-scaled links [10] aim to improve the energy efficiency of the NoC.

Most of these works target efficient packet transfer between the various router nodes of an NoC. To the best of our knowledge, this is the first work to investigate the power variations at an individual router level using multiport routers. Also, we discuss the IR drop effects that arise by using larger multiport routers.

3 Experiment Platform

Exploiting the advantages of a NoC style of interconnection is gaining popularity in FPGA-based SoC designs [5, 23]. In this work, we use the router designs that were originally developed for an FPGA-based NoC. Hence, in our experimental flow, we carry out the prototyping and characterization of router modules on an Xilinx-based FPGAs to meet the first objective.

Xilinx Flow: In this flow, the power differences present between various pairs of ports in a multiport router are captured. We obtain the primary multi port router designs from [20], which are based on Xilinx FPGAs and make intelligent use of the block RAMs available across the FPGA. As shown in Figure 1, given the port count and the target FPGA device, we synthesize the various multi port designs using the Xilinx ISE synthesis tool. After the Place-And-Route phase of synthesis, we simulate the Placed-And-Routed (PAR) router simulation model using ModelSim 6.3i [16] and generate the Value Change Dump (VCD) file. Throughout the simulation, the switching activity of all nets and logic in the PAR design at every clock step are stored in the VCD file. Next, XPower tool of the Xilinx ISE 6.3i [29] is used to obtain the power estimate values of the design, for the vectors that were provided as input for the current run. XPower takes in the PAR design file (.ncd), the physical constraint file (.pcf), the user settings file (.xml) and VCD file (containing the activity data) and provides an estimate of various power parameters. We use the ff896 package of XC2VP30 Xilinx Virtex II Pro FPGA for the purposes of power estimation. For experimentation purposes, the temperatures including the ambient and junction temperatures

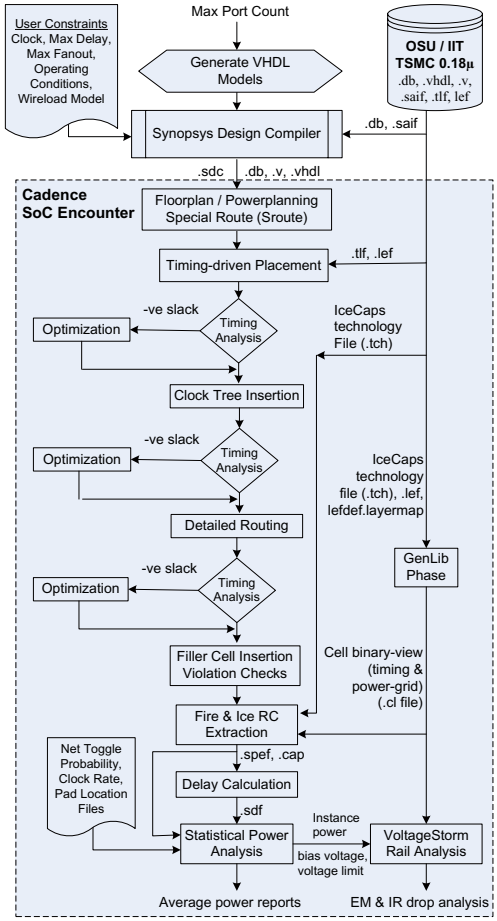


Figure 2. Synopsys-Cadence Flow

are set at 25 degree celsius during all simulation runs.

Synopsys-Cadence Flow: A vector set is used to observe the power variations between various ports in the Xilinx FPGA based flow. Though the power estimation tool (XPower) of the Xilinx ISE synthesis platform is able to report the average and peak powers, it is not comprehensive in terms of the temperature and IR drop analysis. Many of the device level details are abstracted away and the user has to remain contended with the summary reports and files generated by Xilinx ISE. Due to limited leeway available for an extensive IR drop analysis, we port the designs onto a ASIC based flow, making use of the Synopsys and Cadence CAD tool set. During porting, the only required change was to replace the Xilinx BRAM based FIFO (the buffer elements that store the packets in an NoC) association into a user defined FIFO . This is because the Synchronous FIFO implementation using BRAM is only available as a black-box implementation using Xilinx LogiCORE tool [28] and the corresponding reference is replaced with a new RTL implementation of the FIFO.

Figure 2 shows the complete flow for layout synthesis, followed by power and rail analysis. TSMC 0.18μ library available from OSU (formerly from IIT) [2] is used at various stages of the flow. First, the VHDL router designs are

Source Port	# Destination Ports receiving the same data from Source port											
	1 (1-to-1 transfer)			2 (1-to-2 transfer)			3 (1-to-3 transfer)			4 (1-to-4 transfer)		
	Average Power (mW)			Average Power (mW)			Average Power (mW)			Average Power (mW)		
	Min	Max	Avg	Min	Max	Avg	Min	Max	Avg	Min	Max	Avg
N	173	180	177.75	186	190	187.70	193	197	195.20	201	204	202.20
E	190	194	192.13	200	204	203.30	210	216	212.70	220	224	222.00
W	162	165	163.75	172	177	174.90	182	188	184.80	193	197	194.80
S	153	163	159.63	170	174	172.10	180	184	182.00	190	193	191.80
L0	171	175	172.50	178	181	179.50	184	187	185.75	192	192	192.00
L1	176	179	177.63	184	187	185.67	192	194	193.00	200	200	200.00
L2	176	182	179.38	185	190	187.50	193	198	194.75	202	202	202.00
L3	172	175	173.50	179	174	179.83	193	197	195.20	193	193	193.00
L4	180	183	181.38	188	192	189.83	196	199	197.50	205	205	205.00

Table 1. Five port router - Average Power consumption between different of ports (L0-L4 represent logic port)

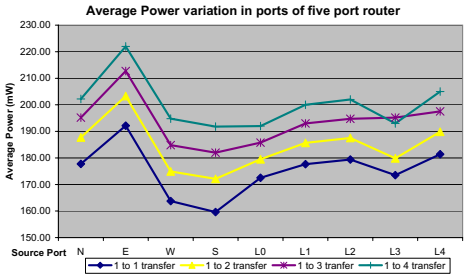


Figure 3. Avg. power in different source ports

input into Synopsys Design Compiler and a gate level net list along with the timing constraint file (.sdc) are obtained. We port them into Cadence SoC Encounter in addition to the timing library (.tlf) and LEF (Library Exchange Format) files of the standard cells from IIT TSMC 0.18μ library. After initial floorplan and power rail (vdd/gnd) definition, the power track routing (special route) and via-insertion are performed. Timing-driven placement, clock tree insertion and detailed routing constitute the next phase of tasks, with the intermediate timing violations removed through an optimization phase. This is then followed by filler-cell insertion and verification, in order to check for various issues including a check for complete connectivity.

The next sequence of steps constitute the power and IR drop analysis using Cadence SoC Encounter [7]. Using the Layer Map file and IceCaps technology file (.tch file, having models for resistance and capacitance extraction in various layers) as input, the GenLib routine is invoked to create a binary-view (.cl library) of the LEF cells (TSMC 0.18μ). The binary view has two key data, namely, the graycell data (for extraction-for-timing flows) and power-grid view of all cells. Fire & Ice RC extractor [1] is used to generate the Standard Parasitic Exchange File (.spef) followed by the delay estimation (SDF file generation). Since, the worst case for IR drop is hard to construct using vector based power analysis, we make use of the statistical power analysis with a net toggle probability of 0.5 and clock rate of 100MHz (typical). A report for average/peak power is generated along with detailed instance power files, which are input to the VoltageStorm tool. VoltageStorm is sign-off tool for detailed rail analysis to find IR drop violations in the layout and the profile is displayed as a power graph [8].

4 Power Savings in Multiport Routers

In a traditional Networks-on-Chip design, a mesh based topology comprises of a router that has four directional ports (North/East/West/South) and one logic port to which the IP core gets attached. This is referred as single (logic) port router. Hence, not counting the directional ports, multiple number of logic ports constitutes a multiport router. A detailed discussion of the router design and capabilities can be found in [21, 20]. Given a topology comprising of multiport routers, the mapping algorithm will cluster the cores optimizing the overall power/performance, while satisfying the bandwidth constraints at the system level [21, 22]. The authors assume that once a mapping is produced, the power for intra-router switching (between ports of the same router) remains the same. Hence, on an individual router basis, the logic port to which core gets attached is not considered.

In this work, we concentrate on the multiport router and analyze the power differences in switching packets between various ports (intra-port transfers). We simulate the router designs by switching a *fixed set* 10000 packets between various router ports. Table 1 summarizes the average power estimated by the Xilinx XPower tool for different combinations of packet transfers between various ports. Each row corresponds to a source port from which the packets are switched to multiple ports in a multicast fashion * [20]. Each source port can switch to any combination of the rest of the ports. Eg., in first case, N can transfer to {E, W, S, L0, L1, L2, L3, L4} and in 2nd case N can transfer to {L0&L1, L0&L3, L0&L4, L1&L2, L1&L3, L1&L4, L2&L3, L2&L4, L3&L4, ...}. Similarly, combinations for rest of the cases and for rest of the source ports can be obtained. Owing to verbosity, for each of the four cases & for each of the source port, we present the *minimum*, *maximum* and *average* of all the combinations of transfers.

For a given source port, the *minimum* and *maximum* values clearly indicate the spread of the average power consumed based on the destination port(s) at hand. Contrastingly, the choice of source port also affects the average power, as shown in Figure 3. For instance, in case I (1-to-1 transfer), the difference in average power based on the source port is as high as 20% (refer 4th column of Table 1). Assuming the degenerate case wherein same amount of data is switched between all ports, the minimum savings of 20% is obtained. Depending on the amount of data that is switched between ports by an application in hand, the savings can grow to a large value. It is seen that irrespective of the type of transfer (1-to-1/1-to-2/1-to-3/1-to-4), W & S & L0 are better candidates as source ports for a high bandwidth transfer, with E & L4 being worse.

After developing a database of power values for various ports of a multiport router, a power-efficient mapping on a per router node basis is possible by careful selection of ports during the mapping phase of NoC. Thus, it is clearly seen

*The four cases indicate the number of participating ports which receive the same data from the single source port (multicast) [20].

that the choice of the source port and the destination port is of prime importance for improving the power efficiency of an NoC having multiport routers.

5 Power Issues in Multiport Routers

In this section, we analyze the power-related issues that arise owing to a complex/larger multiport router, using the Synopsys-Cadence flow for the various simulation runs. In addition to statistical power analysis, an exhaustive rail analysis is performed to observe the negative effects in terms of IR drop increase [4, 25, 32].

(1) Average Power Increase: Addition of ports to a router reduces the dimension of the topology of the Networks-on-Chip, since the routers with smaller port count are replaced with a larger multiport router. Albeit a reduction in the operating frequency, the overall system performance and power improves as lesser hops take place [21]. But, a power perspective of larger multiport router needs to be established to find the point of diminishing returns for average power.

Figure 4 shows an increase in the average power that results due to addition of ports forming a larger multiport router. The flatness of the curve with changing toggle probabilities for the *same router* design is along the expected lines. With respect to the average power of a single port router, we observe an increase as high as 5× in case of nine port router (refer br9inc in the figure). For an overall power efficiency, this increase in average power must be less than the power gains obtained by hop reduction using a multiport router in place of multiple smaller routers.

A 3×3 mesh (with 9 single port routers) and different multiport routers are shown in Fig. 5. Using data from Fig. 4, the increase in power with respect to the single port router is indicated inside the boxes of all the router versions (Fig. 5). For example, the increase in the average power of a three port router is 1.3×. It takes approximately 20% more power to switch a packet between two routers compared to the packet switching within a router (between various ports) and hence the links (assuming equal/uniform links)s connecting the various single port routers in the 3×3mesh are annotated with a 1.2× increase [24].

Let us assume a simple case where there is a single source and other routers receive from the source (marked as D1-D8 in 3×3 mesh). The total power is the summation of the power at various links and ports of the routers. For instance, in a 3×3 mesh having 9 nodes (1 source (S) and 8 destinations), S-to-D1 & S-to-D2 consume 2.2× (1.2+1), S-to-D3, S-to-D4 & S-to-D5 consume 3.4×(1.2∗2 +1) , S-to-D6 & S-to-D7 consume 4.6 (1.2∗3 +1) and S-to-D8 consumes 5.8× (1.2∗4+1). Note that all of them have a constant single additive term of 1 (the average power of a single port router) representing the power required to switch to the logic module, on reaching the destination router. In total, it takes 29.6× to send one packet from the source to all of the 8 destinations. In contrast, if we have a single nine port router, the total power required is estimated as 40× (8 packets ∗ 5×), since the average power is 5× compared to a single port router.

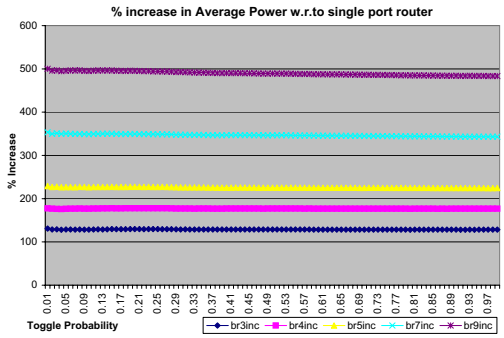


Figure 4. Average Power increase

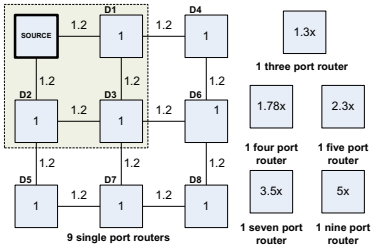


Figure 5. Example NoC mesh with Normalized Power Values

Table 2 summarizes the results for other router versions using the above method. When using only the single port routers, prime & odd number of routers introduces a linear chain of routers. For example, 1×3 mesh for 3 routers, 1×5 mesh for 5 routers and 1×7 mesh for 7 routers, the diagonal length of which are abominably high. Case I in Table 2 represents the power increase tolerating this linear chain. This linear chain can be broken, provided the router count is even. We can render it possible by using a two port router in place of two single port routers. Thus, we can transform 1×3, 1×5 and 1×7 linear chains into 1×2, 2×2 (grey-shaded inside dotted box) and 2×3 meshes, thereby, reducing the diagonal length by half. Taking this new scenario into account, Case II of Table 2 represents the effective power increase†. We can observe that a single nine port router is inferior and a seven port router is bad compared to the Case I (linear chain) in terms of the power. Even though a combination of smaller multiport routers (eg., 2-5 port routers) is beneficial, a larger multiport router (eg., 9 port router) must be sparingly used from a power angle.

(2) Rail Analysis: A router is a combination of various elements including buffers, I/O channels and a crossbar based interconnection of various ports. The switching activity is distributed in a non-uniform fashion across the router with the crossbar bearing the brunt. This is particularly true inside a crossbar where a complex interconnection of multiplexers and demultiplexers between various ports increases the interconnect density and hence the switching activity,

†It is assumed that the new two-port router is at the source and hence, one of the transfers is an intra-port transfer requiring 1.2× power.

# nodes	using single port routers		using one multiport router
	Case I	Case II	
3	5.6×	3.4×	2.6×
4	7.8×	-	5.34×
5	16×	9×	9.2×
7	31.2×	17×	21×
9	29.6×	-	40×

Table 2. Increase in Average Power normalized w.r.to a single port router

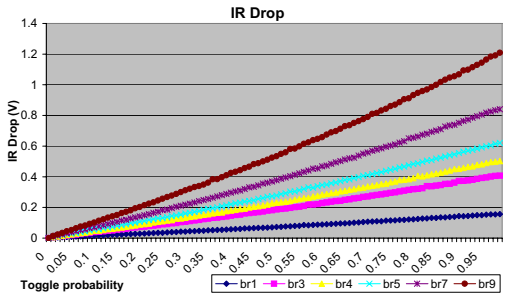


Figure 6. VoltageStorm Rail Analysis - IR drop in various routers

within a small area. Concentration of large switching activity on the crossbar results in large current being drawn from the nearby rails. Such non-uniform IR drops introduce large variations in temperature gradient, creating hotspots in extreme cases [6]. The non-uniformities of temperature across the substrate is shown to degrade the interconnect performance [4]. Hence, timing issues are created due to excessive IR drop and ground bounce effects. Recent articles throw more light on the importance of doing an extensive IR drop analysis at a post-layout stage for maintaining system reliability [25]. Thus, ensuring the power integrity is of utmost importance in order to prevent chip failures resulting due to thermal and electromigration effects [32].

The issues discussed above are exacerbated by the arbitrary addition of ports in order to realize a larger multiport router. In a large SoC, concentration of high switching logic design is detrimental due to various thermal-related issues. Hence, we do an extensive rail analysis of the various multiport router designs, using the sign-off rail analysis tool, VoltageStorm of Cadence SoC Encounter [8, 7].

Figure 6 shows that the rate of increase in IR drop with increasing activity inside the router is very large for the seven port router (br7) & nine port router (br9). A similar effect is evident in Figure 8, wherein the % increase in IR drop of various multiport routers is shown with respect to the IR drop of the single port router for various toggle probabilities. In Figure 9, we compare the percentage increase in IR drop of various router designs with respect to the corresponding base design. Here, for a given router design, a base design is the one having the typical minimal value of 0.1 as the toggle probability. For example, for a five port router (br5), the corresponding base design is the IR drop estimated for the same five port router, with 0.1 toggle probability. Till the port count of five, the % increases are uniform with the curves overlapping. But, the deviation

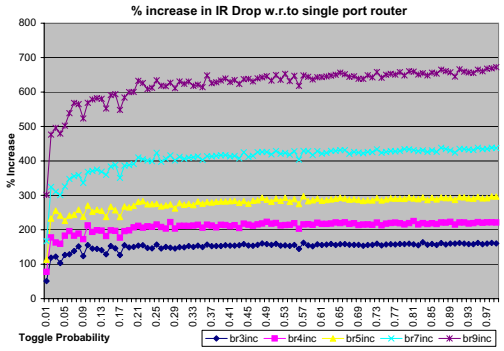


Figure 8. VoltageStorm Rail Analysis - % increase in IR drop w.r.t single port router

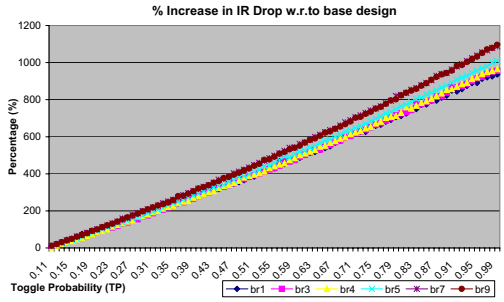


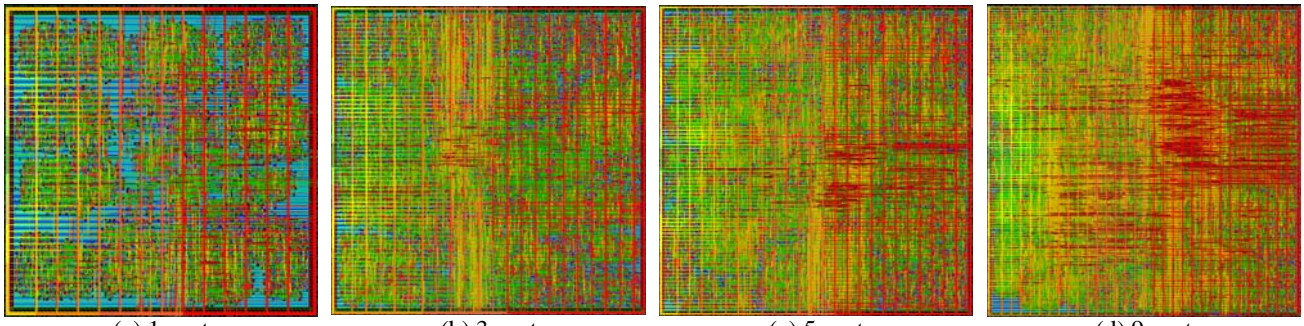
Figure 9. VoltageStorm Rail Analysis - % increase in IR drop w.r.t base design (having 0.1 toggle probability)

is distinct for the seven and nine port cases.

Next, we use the VoltageStorm signoff tool to perform a detailed rail analysis for violations and display the results as a color-coded power graph of the router designs. As suggested in the industry flow [25], we fix the net toggle probability at 0.5 and a clock frequency of 100MHz (typical). In Figure 7, we present the power graphs of selected router versions, showing the violations occurring at various points of the router designs (as determined by VoltageStorm). As we move from left to right, we notice a marked increase in the amount of violations, the worst being indicated by dark red color. As pointed earlier, the worst violator regions happen to the ones having the crossbar connections. This distribution of IR drops is a good indicator of the temperature gradient profile that will result across the substrate [25, 8].

6 Conclusion

Application-specific NoCs target custom tailoring of topology using multiport routers. Given this scenario, we analyze the merits and shortcomings of multiport routers from a power perspective. By exploiting the switching power differences among the various ports, it is possible to achieve a power-efficient mapping. Through exhaustive rail analysis, we observe that large multiport routers introduce greater amount of IR violations. In summary, we infer that a heterogenous mix of smaller multiport routers will provide a better tradeoff in terms of performance and power.



(a) 1 port (b) 3 port (c) 5 port (d) 9 port

Figure 7. VoltageStorm Rail Analysis (IR drop) power graphs - *Color illustration*

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